PHYSICAL UNDERSTANDING OF STRAINED-SILICON AND SILICON GERMANIUM FETS FOR RF AND MIXED-SIGNAL APPLICATIONS

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PHYSICAL UNDERSTANDING OF STRAINED-SILICON AND SILICON GERMANIUM FETS FOR RF AND MIXED-SIGNAL APPLICATIONS

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Dedicated to the Divine's Creation

Bliss, Love & Joy

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

The objective of proposed research is to investigate the potential of strained silicon and silicon-germanium (SiGe) based devices for RF/mixed-signal applications. Different device topologies, namely strained buried channel modulation doped field effect transistor (MODFET) and silicon-on-insulator (SOI) based MOSFETs, are studied in this context. Our preliminary results on SiGe MODFETs indicate strong dependence of device performance on displacement damage, which is critical for extreme environment applications. This research will be an effort towards understanding the physics of these devices in extreme environment conditions.

CHAPTER 1

INTRODUCTION

1.1 Motivation

There has been unprecedented growth in global telecommunications market during the recent years. Due to the exploding product marketplace, the technology of choice is delineated by a complex boundary of cost and performance, which changes with time. The wireless consumer application space is now being dominated by silicon-based technologies, which once used to be a niche GaAs market. For example, the growth of mobile communication (GSM/CDMA), WLAN, and GPS markets has been primarily driven by advances in silicon based technologies which allow single chip integration, reducing cost and system size. Even though SiGe BiCMOS processes offer better RF/mixed-signal performance and foundry integration with CMOS process, RF CMOS technologies would still be the optimal choice where the SiGe HBT performance is not fully required and cost is paramount. Various RF technology options available are mapped into the overall application spectrum in Figure 1. The acceptable range of cut-off frequency is chosen as 3X-10X of the application frequency.

RF CMOS technology can be considered as an enhancement on the basic digital process with improved RF models, design automation, and passive devices built from the existing base process. Some processes offer a higher resistivity substrate (without an extra mask step) and triple-wells with standard CMOS process to improve RF isolation. The important circuit performance metrics for these applications are low power consumption, high frequency operation, high dynamic range, good linearity, low noise, and high gain. These circuit level metrics eventually couple to the device level metrics which necessitates the understanding of key RF performance metrics of state-of-the-art technologies at a device level.

Extreme environment high speed communications is another niche market with applications in extra-terrestrial environments (space missions), oil exploration, automotive environments, and military applications. The two foremost challenges for extreme environment electronics are radiation hardening and their ability to perform across wider temperature ranges. The primary goal of this thesis is to provide insight into the physical mechanisms governing RF performance metrics of advanced SOI CMOS technology and silicon-germanium based MODFET technology, particularly for extreme environment applications. We investigate the radiation response and responsible damage mechanism in these devices in subsequent chapters. Transistor level *dc* and *ac* measurements coupled with parameter extractions are employed to observe the induced effects. We will discuss the SiGe MODFET device technology and state-of-the-art 65nm SOI CMOS technology in subsequent sections of this chapter. Our studies are performed in the context of these two technologies.

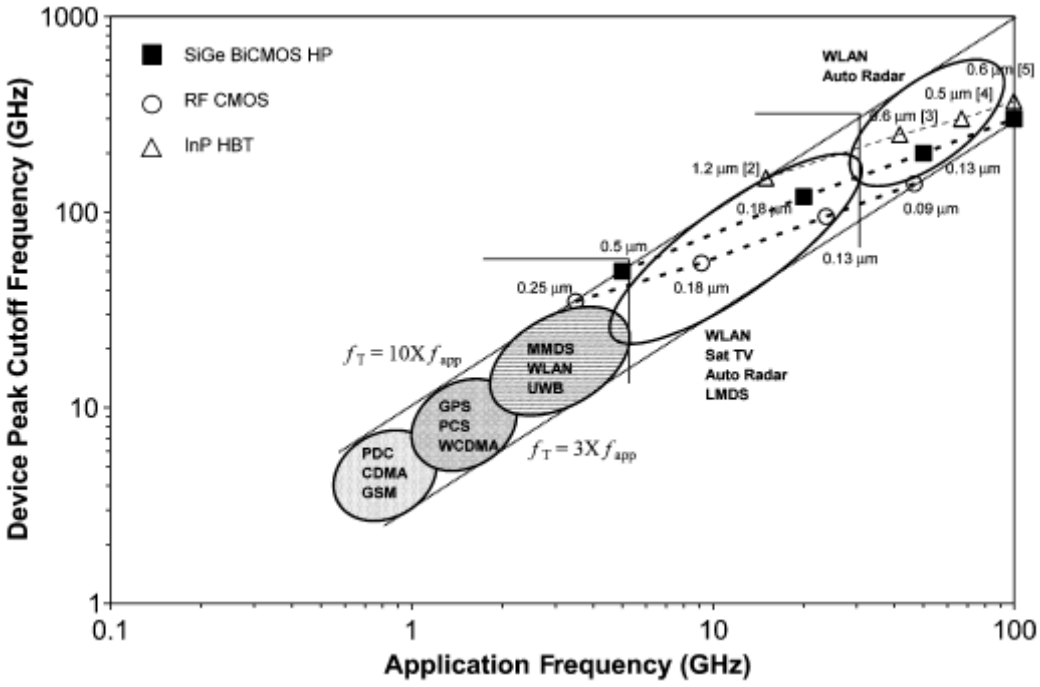

Figure 1: Mapping of technology performance with RF application spectrum [1].

1.2 Silicon-Germanium MODFET

Bandgap-engineered strained-Si/SiGe n-MODFETs or high electron-mobility transistors (HEMTs) are promising candidates for future RF and mixed-signal circuit applications [2], [3]. They provide high performance at low cost by offering compatibility with standard CMOS logic processes. Their demonstrated mobility advantage at low drain voltage and current levels compared to conventional CMOS makes them very attractive candidates for high speed and low power applications [4]. Currently, impressive levels of device performance have been achieved.

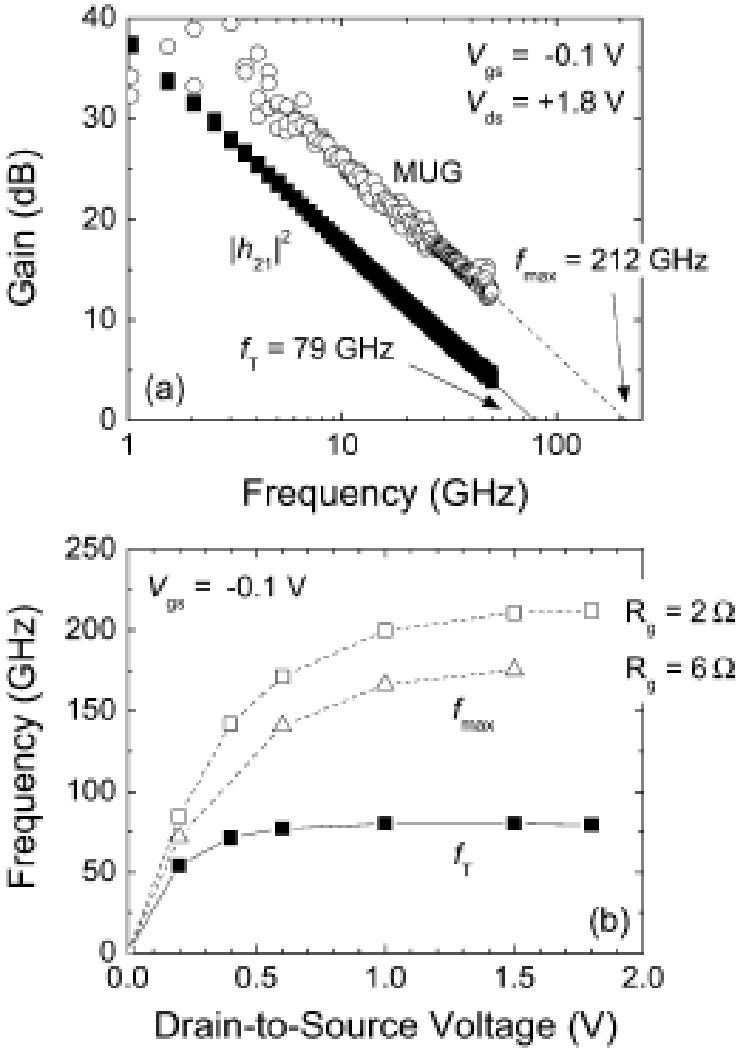

Figure 2: SiGe n-MODFET demonstrates f_{MAX} > 200GHz at L_G = 70nm [5].

Figure 2 shows that an f_{MAX} of 212 GHz has been obtained for SiGe n-MODFETs at gate lengths of 70nm. The buried channel nature of these devices also ensures that they offer lower flicker noise compared to CMOS. The potential compatibility of Si/SiGe MODFETs with traditional silicon-based wafer manufacturing, and the ability to achieve complementary device topologies (n-MODFET + p-MODFET = C-MODFET) on the same silicon wafer [6], [7], differentiates Si/SiGe MODFETs from their III-V counterparts.

Figure 3 shows a schematic cross-section of the Si/SiGe n-MODFET investigated [5]. The source-to-drain length (L_{SD}) is defined to be the distance between the source and drain implants. Devices with gate lengths (L_G) ranging between 70nm and 100nm and L_{SD} ranging between 300nm to 800nm were used for our experiments.

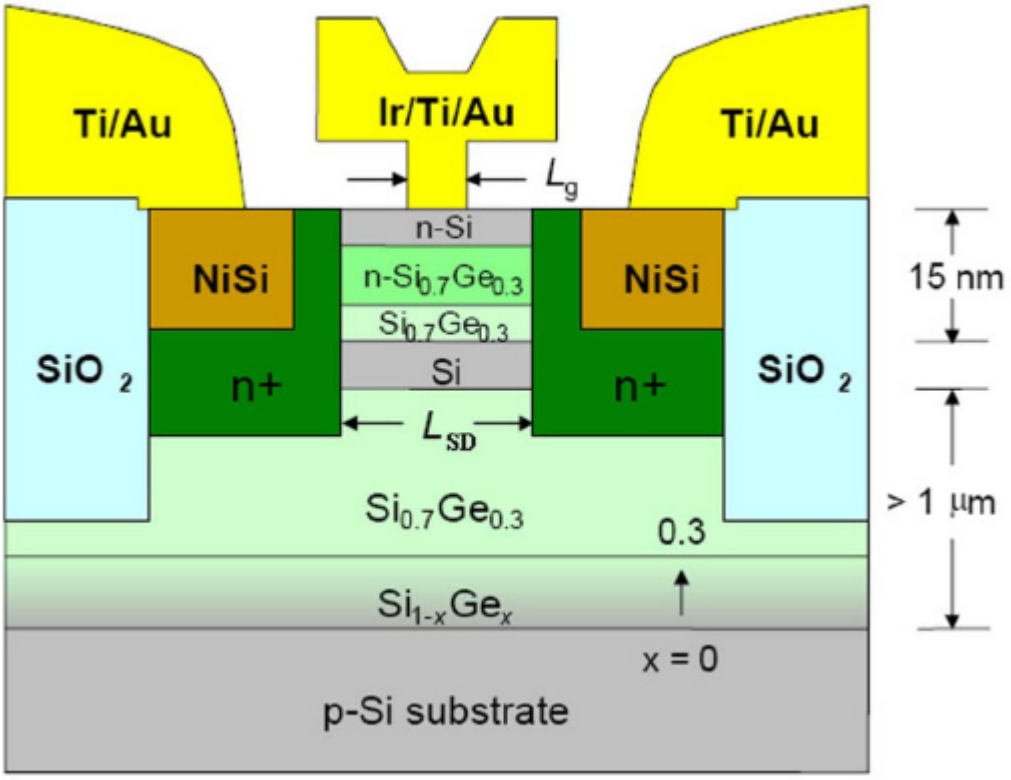

Figure 3: Cross-section schematic of the Si/SiGe n-MODFET [5].

Device isolation was first performed using SiO_2 filled shallow-trench. After performing resist openings, a germanium pre-amorphization implant was completed. Phosphorus ions were subsequently implanted with a dose of $5x10^{15}$ cm^{-2} at an energy of 12 keV. The rapid thermal activation of implants was carried out at 700ºC for one minute. Contact silicides were formed by deposition of SiO_2 and TiN, patterning of resist, and etching the TiN and SiO in the patterned regions. This was followed by sputtering of 12nm of Ni and 20nm of TiN and subsequent annealing step at 500ºC for one minute. The NiSi regions were offset by 100nm from the edges of source and drain implants. A buried silicon channel is formed, enclosed by $Si_{0.7}Ge_{0.3}$ layers on both top and bottom, and the entire channel structure is grown on a step-graded SiGe relaxed buffer layer using ultrahigh vacuum chemical vapor deposition (UHV/CVD). The conduction band offsets at the Si/SiGe interface provide electron confinement for carriers in the silicon channel, as depicted in Figure 4.

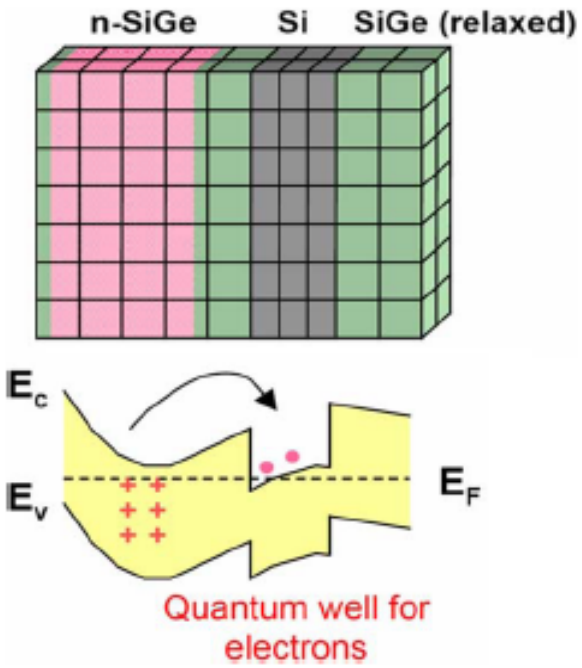

Figure 4: Silicon layer enclosed between the SiGe layers forms the quantum well channel [8].

The T-shaped Ir/Ti/Au gates were patterned using electron beam lithography which involved patterning of dual layer resist, followed by evaporation and lift-off of the Ir/Ti/Au metal. The gate stack was not self-aligned to the source and drain [5]. Figure 5 shows a TEM image of the Si/SiGe n-MODFET fabricated with a metal T-gate.

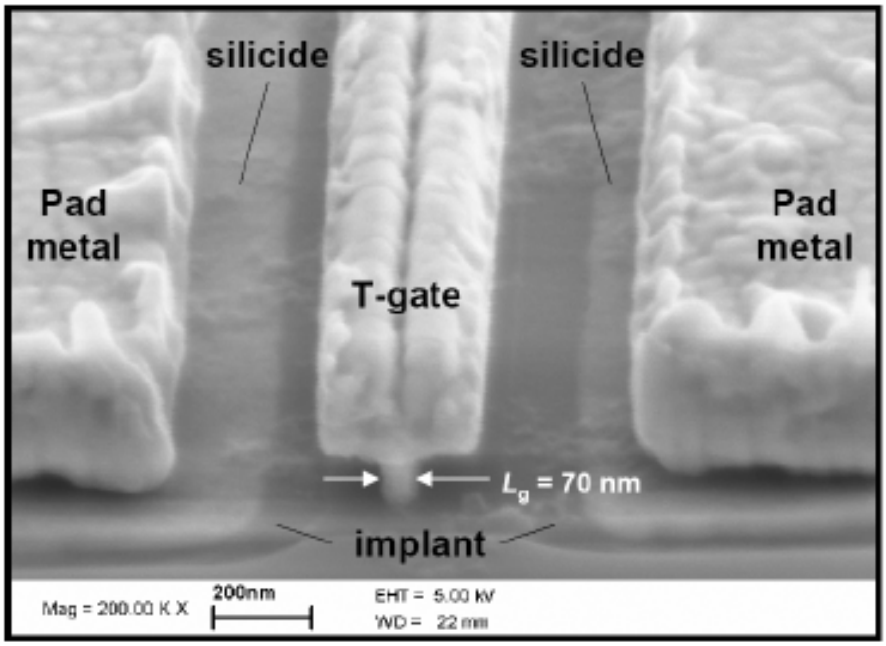

Figure 5: TEM of a SiGe n-MODFET showing the T-gate structure with L_G = 70nm and L_{SD} = 300nm [8].

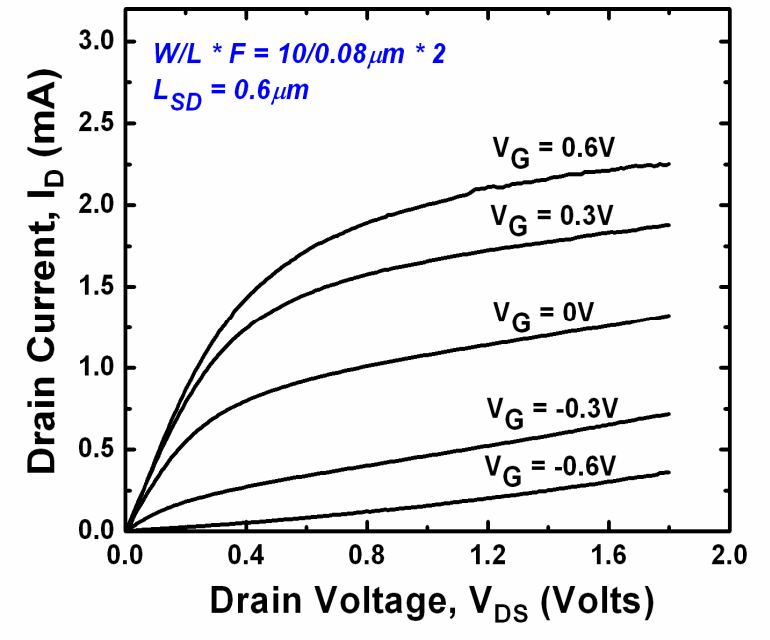

Figure 6: Output Characteristics of strained-Si/SiGe n-MODFET [8].

The measured *dc* output characteristics of a typical MODFET with L_G = 80nm and L_{SD} = 600nm are shown in Figure 6. Significant drain currents are obtained at low drain bias due to the mobility advantage offered by the buried strained silicon channel. The g_m advantage at low drain bias can be seen through the enhancement of the f_T metric as seen in Figure 7. The bias dependence of f_T in SiGe n-MODFET device was compared with Si MOSFETs. The MOSFETs used for this study were partially depleted SOI MOSFETs with L_{poly} = 0.13µm. This gate length was chosen since it produced devices with an f_T similar to that of MODFETs at V_{DS} = 1V. The gate bias for both devices was chosen to establish the peak f_T. From the figure, it is evident that at lower V_{DS} (~0.25V), the MODFET f_T is 30% higher than the MOSFET, while at V_{DS} = 0.1V, the f_T improvement increased to about 50%.

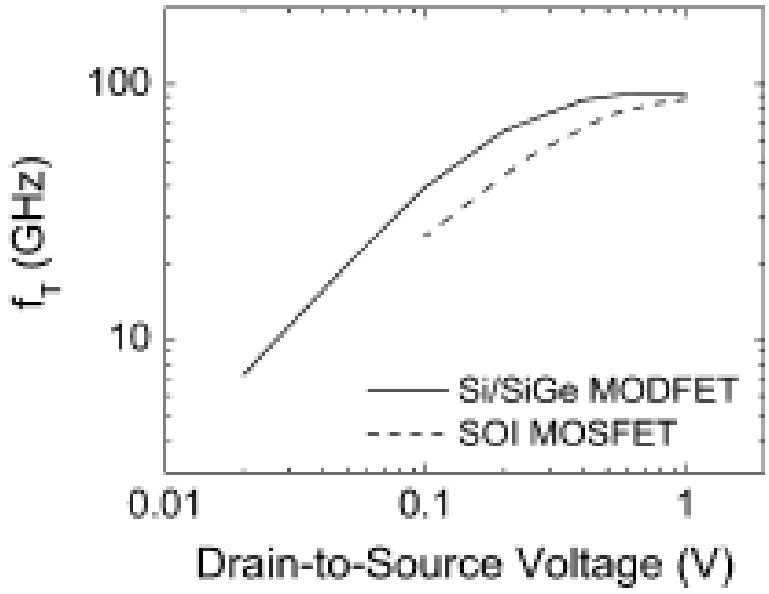

Figure 7: Peak f_T comparison of a Si/SiGe n-MODFET with SOI MOSFET of similar performance [5].

Further device optimization challenges in SiGe MODFETs have been studied through the use of device simulator [9]. It was observed that if both lateral and vertical dimensions are scaled properly, significantly higher f_T (>300 GHz) may be achieved with acceptable DC voltage gains (>10) as shown in Figure 8.

Thus, the potential of SiGe MODFETs for high-speed, low power operation is substantial. However, a considerable improvement in MODFET device design is needed to obtain competing performance with state-of-the art CMOS technology, which is discussed in the subsequent section.

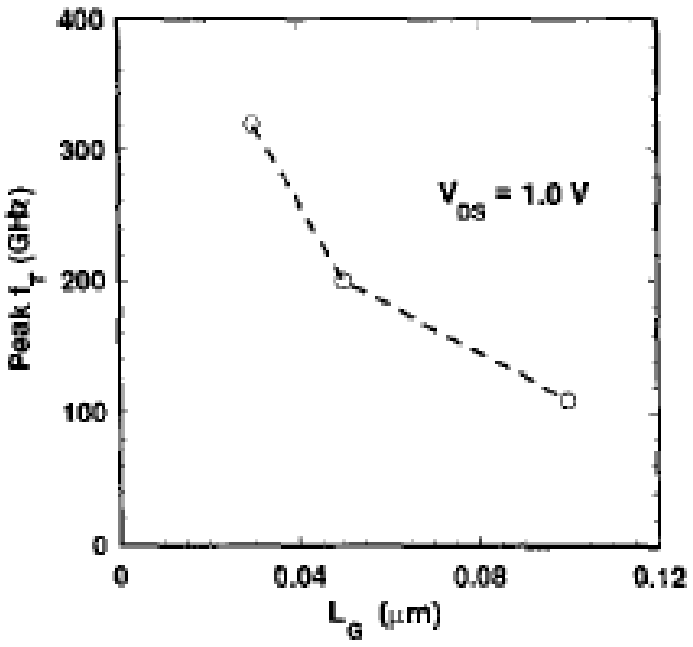

Figure 8: Scalability of SiGe n-MODFET can offer f_T > 300GHz at gate length of 30nm [9].

1.3 Silicon-On-Insulator MOSFET

Impressive performance and density gains have been achieved through CMOS scaling for the past 20 years. However, the definition of ideal scaling has been changed over time in order to maintain performance advantages at each generation. The *ideal* and *reality* scaling scenarios are shown in Figure 9. In contrast to the ideal scaling where all dimensions are scaled by the same scaling factor ($\alpha<1$) to maintain constant electric field from generation to generation, the actual trends have followed a mix of $\alpha^{1/2}$, α and α^2 scaling. The primary reason for this non-ideal scaling is the increase in standby power of CMOS devices, which is not accounted for in an ideal scaling scenario. The decreasing gate oxide thickness and threshold voltage have raised huge concern about standby power, focusing the attention of industry towards a non-ideal or *reality* scaling scenario.

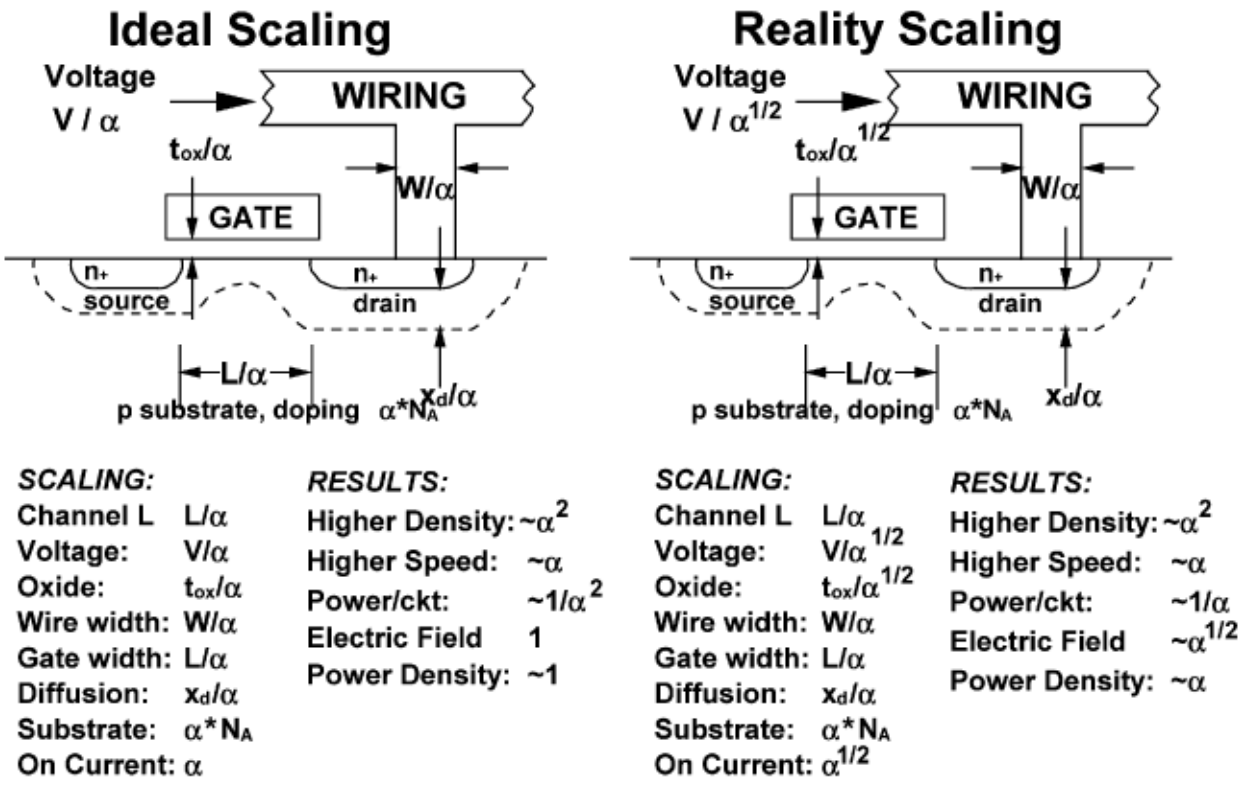

Figure 9: *Ideal* and *Reality* scaling scenarios seen over past few years [1].

Aggressive scaling has also improved the frequency response and potential for using advanced CMOS technology RF applications. RF CMOS technology provides RF enablement to a simple digital CMOS technology, while being the lowest cost adder. A combination of process innovation (e.g. strain engineering) and lithographic scaling is being used to improve CMOS performance. These innovations include SOI substrates, strained silicon layers for mobility enhancement [10, 11], double-gated devices [12], and fully silicided or metal gates [13]. The scaling trends in digital CMOS have had a strong influence on the RF CMOS roadmap. For example, the f_{MAX} scaling and broadband noise can benefit from the lower resistance of fully silicided (FUSI) gates, but the flicker noise may require more attention as new gate oxide materials are introduced [14]. Amongst

available choices, SOI CMOS technology provides added advantages over bulk CMOS technology by minimizing parasitics, improving isolation, decreasing leakage, improving short channel effects, and enhancing single event upset (SEU) tolerance. This performance improvement, coupled with its high-density integration capability, cost effectiveness, and process maturity makes SOI CMOS technology attractive for integrating RF front-ends and the base-band analog and digital circuitry onto a single chip.

We have studied the proton radiation tolerance of state-of-the art 65nm SOI CMOS technology (Chapter 4). The CMOS devices under investigation are available in a fully-integrated 65nm SOI CMOS technology with high Q on-chip inductors and capacitors to enable RF/analog system-on-chip (SoC) applications [15]. A Stress Memorization Technique (SMT) is used for the nFETs where deposition of a stress dielectric film and subsequent anneal enhance tensile strain. The peak f_T's of 360GHz and 260GHz for nFET and pFET were reported at room temperature in Figure 10.

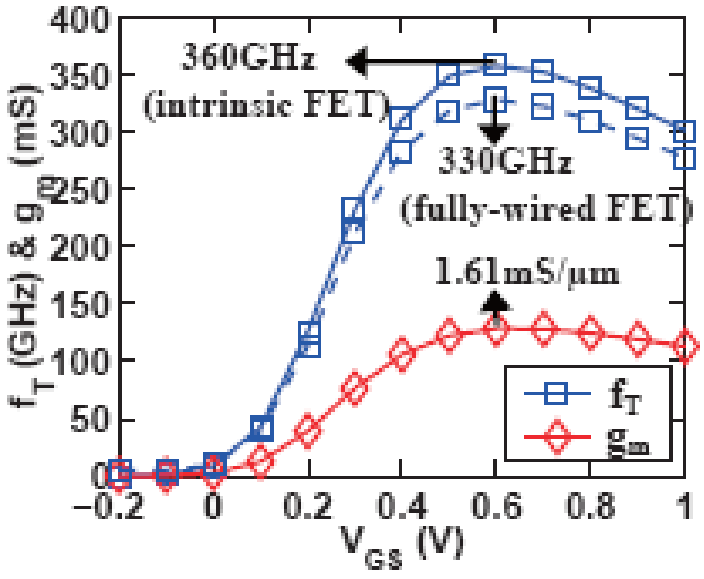

Figure 10: Record RF performance for a 65-nm CMOS technology [16].

Relaxed pitch layout was used in RF devices to improve performance. The twin-well CMOS technology on p-type SOI substrate was designed for a V_{DD} of 1V. Low resistance FUSI gates were implemented and devices are fully oxide insulated by shallow trench isolation (STI) and buried oxide (BOX). For our analysis, we used high threshold voltage, thin gate oxide variants of nFETs. The TEM cross-section of both nFET and pFET are shown in Figure 11.

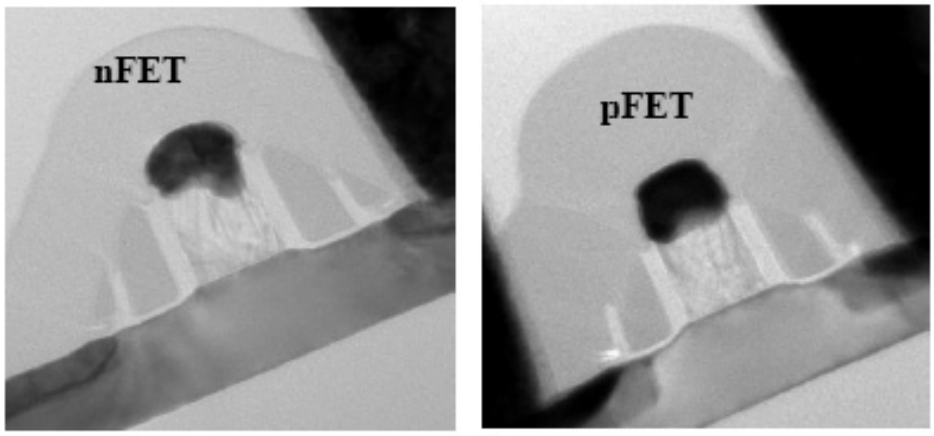

Figure 11: High Resolution TEM cross-section of nFET and pFET available in 65nm SOI CMOS technology [15].

1.4 Summary

In this chapter, detailed description of device technologies i.e. SiGe MODFET and 65nm SOI CMOS was provided. Although SiGe n-MODFETs provide added advantage at low-drain bias over CMOS technologies, careful device optimization is required before establishing it as a mainstream production-ready technology. On the other hand, state-of-the-art 65nm SOI CMOS technology provides RF performance benefits with scaling. Devices with peak f_T performance of 360 GHz have been demonstrated.

In subsequent chapters, we investigate the low-frequency noise of these devices and their radiation tolerance for niche applications such as space mission,

military applications, and other extreme environments where robust RF and mixed-signal products are used. Chapter 2 describes the low-frequency noise and the underlying mechanism in SiGe n-MODFET. While Chapter 3 talks about radiation tolerance of SiGe MODFETs, we investigate the ionizing damage in 65-nm SOI CMOS technology using proton irradiation in Chapter 4. Finally, Chapter 5 concludes the thesis with suggestions for future work.

CHAPTER 2

LOW-FREQUENCY NOISE IN SILICON-GERMANIUM MODFET

2.1 Introduction

As shown in the previous chapter, SiGe MODFETs have remarkable potential for RF and mixed signal applications. Even though SiGe MODFETs provide high-speed and good power-gain at low drain bias, the noise performance of these devices needs further investigation.

High-frequency wireless circuits and integrated transreceivers incorporate high performance analog and mixed signal blocks such as high-speed data converters, precision op-amps, and various other specialty amplifiers such as line drivers. These building blocks not only require high gain and higher output resistance, but also lower noise (both low-frequency and broadband). Low-frequency noise is an important figure-of-merit for almost all electronic circuits and systems because it determines the lowest detectable signal limit, and high frequency spectral purity of the system. Phase noise is caused by the up-conversion of low-frequency noise to higher carrier frequencies, and enlarges the required channel spacing in RF applications, thereby limiting the number of channels in a communication system. Thus it is of great importance to better understand the physical mechanism of low-frequency noise in potential devices for high-frequency, high-speed applications.

Buried-channel devices are known to have excellent low-frequency noise performance because of the absence of surface transport at the oxide/semiconductor or metal/semiconductor interface [17]. The broadband noise of SiGe n-MODFET has been reported in literature [18]. However, low-frequency noise in these devices has not been

investigated before. In this chapter, we investigate the low-frequency noise in SiGe n-MODFETs and make an attempt towards understanding the underlying noise mechanism. Experimentally the low frequency noise in MODFETs shows a 1/f spectrum down to very low frequencies. This type of process demands some process characterized by a time constant dispersion over a wide range up to very large time constants. The results reported in this chapter have been published in [19].

2.2 Basic Concepts in Low-Frequency Noise

Flicker noise (or low-frequency noise) is existent on all active devices. No universal mechanism for flicker noise has been identified, but the origin of noise is mainly traps associated with contamination or defects. The mathematical expression for 1/f noise invariably contains empirically fitted parameters because of the lack of widely accepted mechanism. The expression for spectral density of flicker noise is given as [20]:

$$\overline{i_n^2} = \frac{K_f I^a \Delta f}{f^b}$$

$\overline{i_n^2}$ = noise current spectral density,

Δf = small bandwidth at frequency f,

I = direct current,

K_f = constant for a particular device,

a = constant in the range 0.5 to 2,

b = constant about unity.

Flicker noise reflects 1/f frequency dependence of noise spectral density if b =1.

The principal noise sources in a FET are thermal noise and flicker noise in the drain current. The flicker noise is often much larger than thermal noise in MOSFETs. This is because the MOSFET is a surface channel device. The fluctuating occupancy of traps in the oxide layer can modulate the conducting surface channel all along the

channel, causing random trapping and detrapping of the mobile carriers in the traps located at the Si-SiO_2 interface and within the gate oxide. An example plot of noise spectral density as a function of frequency is shown in Figure 12. The lower frequency at which the plot is twice its high frequency limit is called the flicker noise corner frequency, which is labeled f_{flk} in the figure. At this frequency, the thermal noise and the flicker noise are equal. For any device, the flicker noise corner frequency can be solved for by equating the thermal and flicker noise components in the equation for total noise. For $f > f_{flk}$, the thermal noise dominates. For $f < f_{flk}$, the flicker noise dominates. In some devices, the flicker noise corner frequency can be as high as 10 MHz. Corner frequency is a very useful means of comparing total noise. All other things held equal, a lower f_{flk} implies less total noise. For example, it is relatively trivial to build bipolar devices whose 1/f corners are below tens or hundreds of hertz, and many MOSFETs routinely exhibit 1/f corners of tens of kilohertz to a megahertz or more.

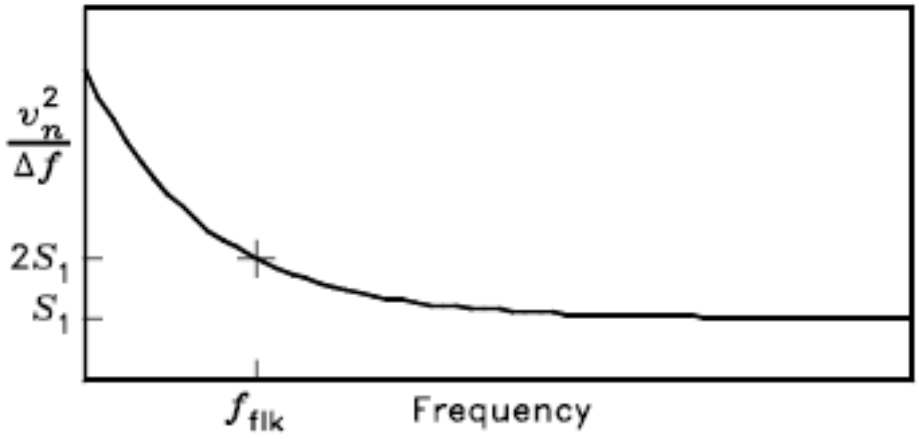

Figure 12: Plot of noise spectral density versus frequency showing the flicker noise corner frequency.

Channel architectures incorporating multiple SiGe quantum well show promising performance improvement when adopted in both PMOS and NMOS short channel transistors, due to increased channel electron and hole mobility [21]. At the same time, better noise performance has been reported [22-27]. Both carrier number fluctuation and

mobility fluctuation [22], [23], [26] have been used to analyze the noise performance improvements in such devices. The attenuating effect from Si-capping layer could be a possible cause for the noise improvement. This is usually attributed to the physical separation of carriers from the surface (oxide interface) and their confinement in the buried channel. Strained-Si/SiGe devices have shown nearly ~10^2 to 10^3 lower flicker-noise levels compared to control silicon devices [28]. Figure 13 shows the noise spectra of buried-channel devices and surface transport devices [17]. It is noticeable that low-frequency noise is reduced by about 17dB in buried-channel devices as compared to surface channel devices. Further work is required to produce transistors having such low-noise performance but with more acceptable circuit parameters, particularly leakage currents.

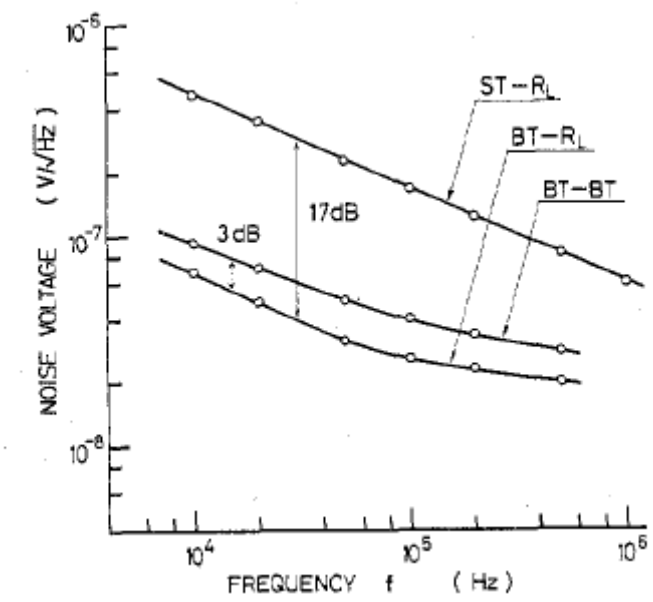

Figure 13: Comparison of noise spectra between optimized buried channel device (BT) and surface channel device (ST). The devices have same W/L value of 8/8 μm, while R_L is 100kΩ [17].

2.3 Low Frequency Noise in SiGe MODFET

The experimental setup used for low frequency noise measurements is shown in Figure 14. This system is in principal the same as [29], but instead of using stepping motors and potentiometers for biasing, an Agilent 4155C Parameter Analyzer is employed. An Agilent 35670A Dynamic Signal Analyzer is used to measure the voltage power spectral density S_{ID}, from resistor R_L, which is series connected with the drain terminal. Noise voltage signals on a metal film drain series resistance were amplified by Perkin Elmer low noise amplifiers (LNA 5113) and fed to the Dynamic Signal Analyzer, covering the frequency range between 1 Hz and 100 kHz. All the instruments are controlled by an external computer through GPIB interface.

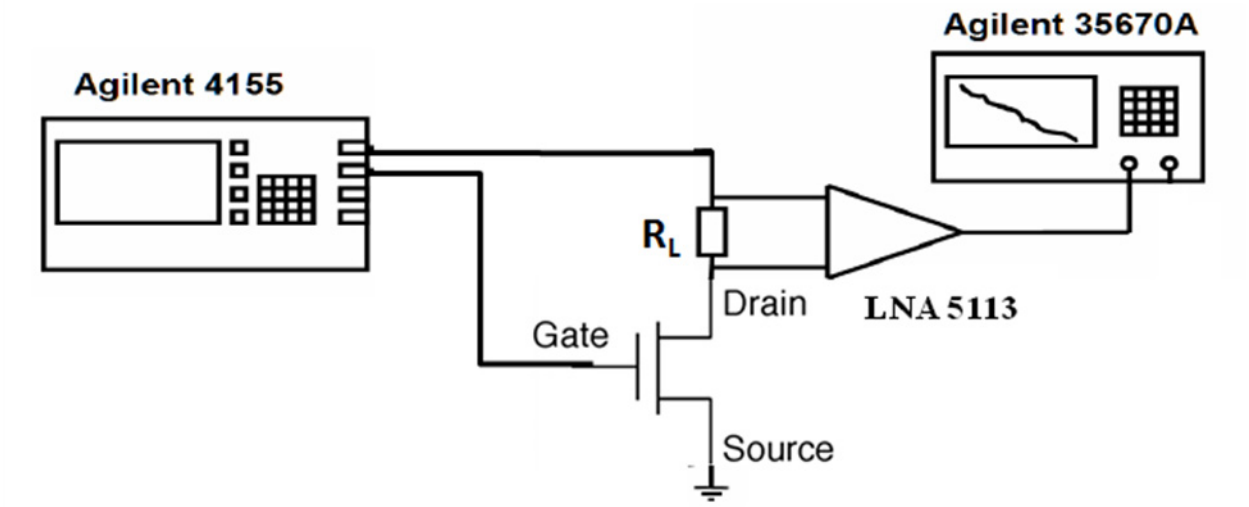

Figure 14: Low-frequency noise measurement setup used to measure drain current noise spectral density. The noise voltage signal on series resistor RL is fed to Perkin Elmer low noise amplifier (model 5113) and measured by Agilent 35670A, a dynamic signal spectrum analyzer. The DUT is biased by an Agilent 4155C Semiconductor Parameter Analyzer.

The drain current noise spectral density is used to probe the underlying low frequency noise mechanisms in SiGe n-MODFETs. Figure 15 shows the noise drain current spectral density of devices with gate lengths of 70 nm and 100 nm, respectively. The noise spectrum shows approximate $1/f^{\gamma}$ dependence. The noise frequency exponent γ was found to vary with bias between 0.95 and 1.06. A small generation-recombination (GR) component is sometimes discernable in the noise spectrum, but the overall deviation of the $1/f^{\gamma}$ fit is small. Figure 16 shows that the impact of scaling of the source-to-drain spacing (L_{SD}) on low frequency noise spectrum is minimal. To identify the microscopic origin of the noise fluctuations, we have used noise measurements in the linear operational region of the device [30]. All further results have been extracted at a frequency of 25 Hz.

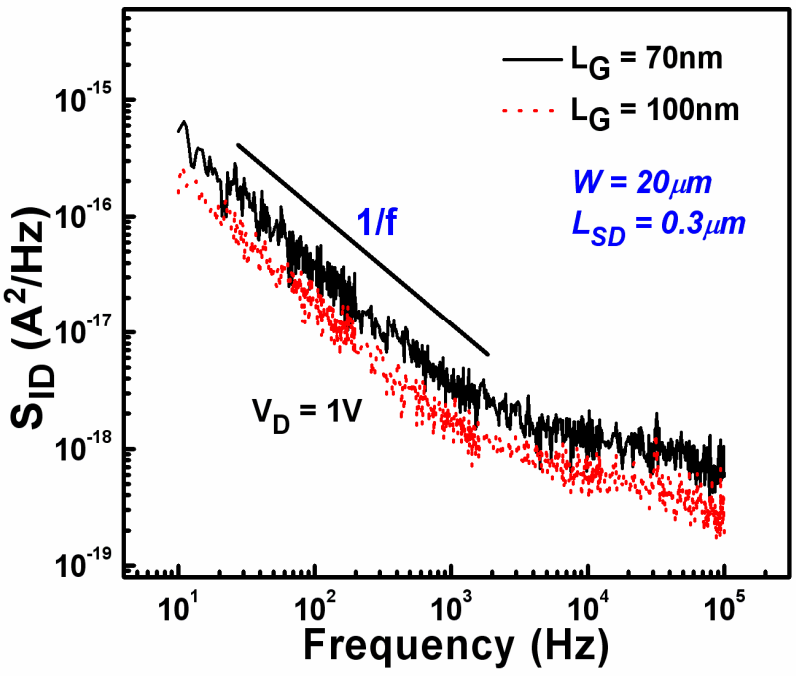

Figure 15: S_{ID} spectrum for different L_G splits of n-MODFETs.

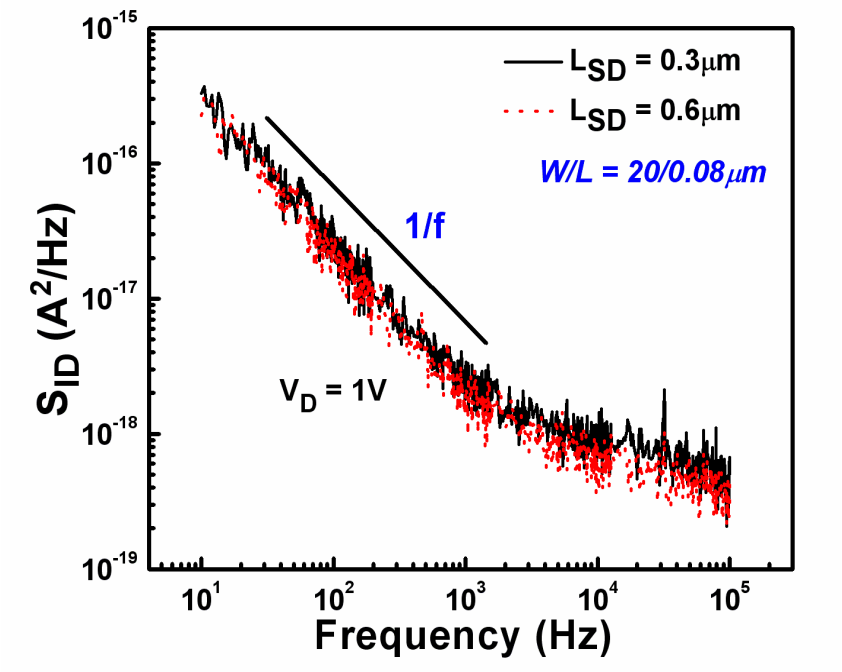

Figure 16: Impact of L_{SD} scaling on S_{ID} spectrum of n-MODFETs.

As shown in Figure 17, the drain current noise shows a peak when plotted against gate voltage, at a fixed drain voltage (50 mV). The bias dependence of S_{ID} is reflected by the corresponding transconductance of the devices. This suggests that the LF noise depends strongly on carrier density and mobility in the channel [31].

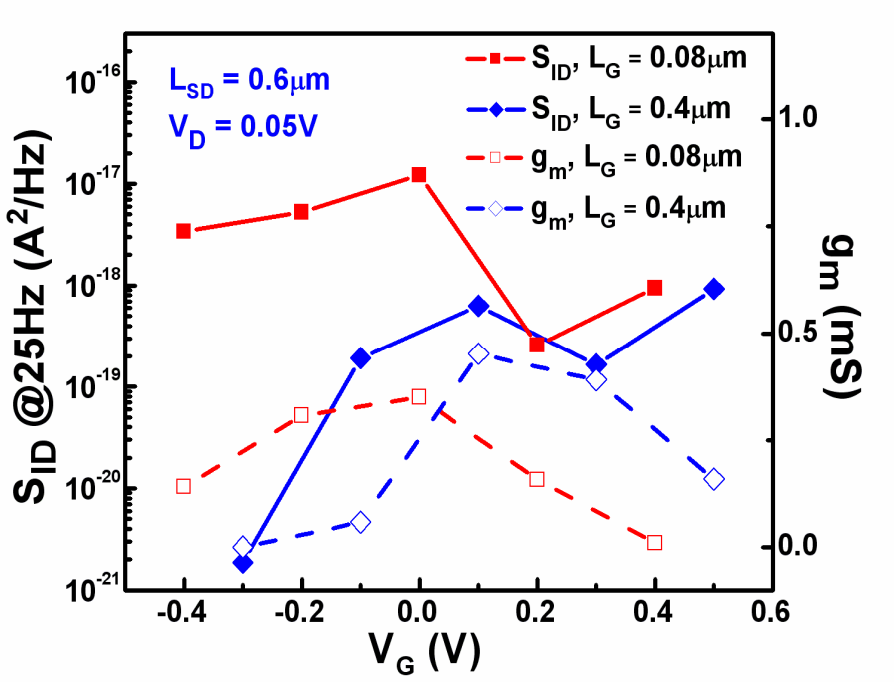

Figure 17: Drain current noise spectral density at constant V_{DS} (50 mV) and the corresponding transconductance at 25Hz for n-MODFETs with different gate lengths.

Figure 18 shows the noise current spectral density dependence on gate length of the SiGe MODFETs. Observe that the S_{ID} magnitude rises as the gate length is scaled. However, a clear trend is not observable for S_{ID} dependence on L_{SD}, as shown in Figure 19. We further analyzed the normalized current noise spectral density, S_{ID}/I_D^2, at a constant frequency, in order to determine the spatial origin of the 1/f noise. S_{ID}/I_D^2 is plotted in the linear region versus the gate overdrive voltage, V_{GS}-V_T [31], and two clearly distinct regions with a V_G^{-1} dependence and a V_G^{-3} dependence are obtained (Figure 20).

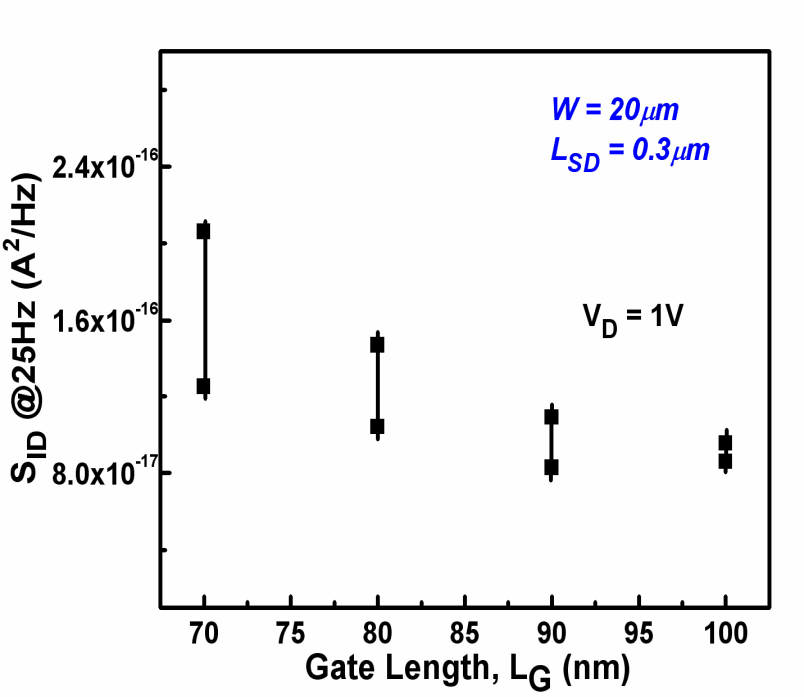

Figure 18: Noise Current Spectral Density (S_{ID}) at 25 Hz for different gate length n-MODFETs.

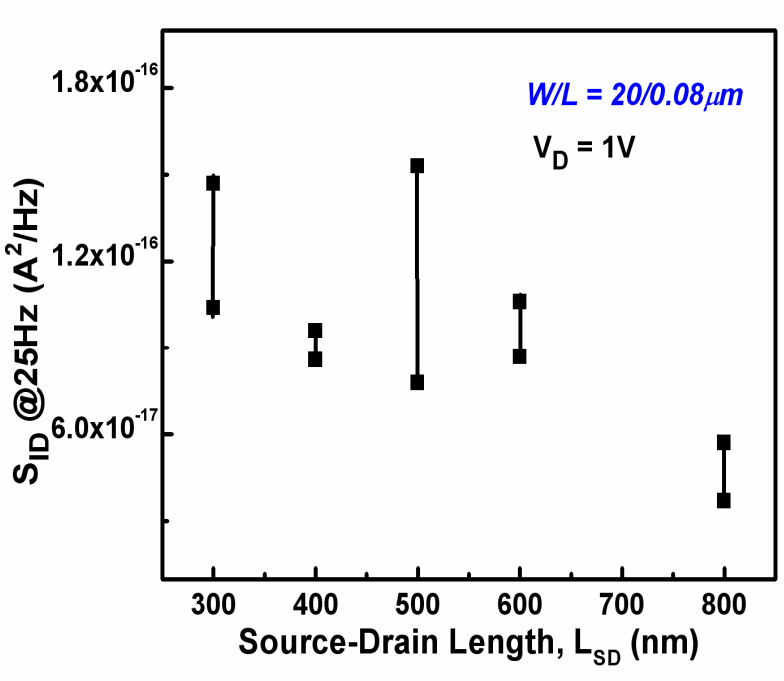

Figure 19: S_{ID} at 25 Hz for different L_{SD} splits of n-MODFETs.

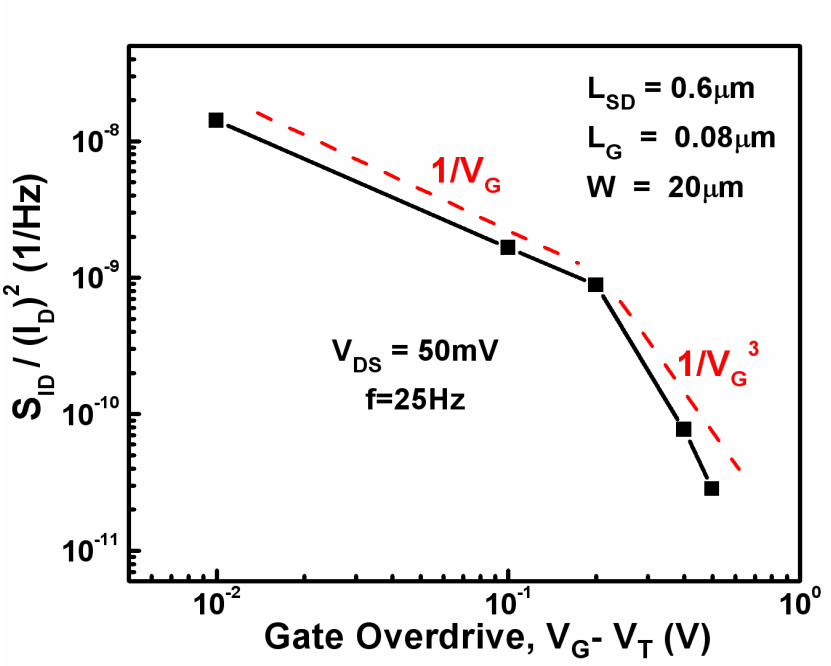

Figure 20: Normalized Current Noise Spectral Density at 25 Hz for a 20 μm x 0.08 μm SiGe MODFET, in linear operation (V_{DS} = 50 mV), as a function of gate overdrive voltage.

The first region corresponds to a dominant R_{ch} region, with the 1/f noise predominantly generated in the channel region under the gate. The second region, with a V_G^{-3} dependence, still corresponds to channel fluctuations dominating the 1/f noise, but R_{SD} becomes greater than R_{ch} [31].

CHAPTER 3

RADIATION TOLERANCE OF SILICON-GERMANIUM MODFET

3.1 Introduction

Chapter 1 highlighted the performance benefits of bandgap-engineered strained-Si/SiGe n-MODFETs for RF and mixed signal applications. The potential compatibility of Si/SiGe MODFETs with traditional silicon-based wafer manufacturing, and the ability to achieve complementary device topologies on the same silicon wafer differentiated Si/SiGe MODFETs from their III-V counterparts.

Radiation-harsh environment is obvious for space missions and military applications. RF and mixed-signal circuits are widely used in many applications in space and military systems. Common to all these applications is the need for radiation tolerance and long operation life under extreme environment conditions. Each of these environments is characterized by its own spectrum of particles and energy distribution. For example, the main source of energetic particles in a space environment are protons and electrons trapped in Van Allen belts, heavy ions trapped in magnetosphere, cosmic ray protons and heavy ions, and proton and heavy ions from solar flares. Roughly speaking, the damage caused by different particles can be divided into ionization and displacement damage effects. Ionization damage, on the one hand, creates free electron-hole pairs by disrupting electronic bonds while displacement damage, on the other, gives rise to atoms which are displaced from their usual lattice site, leaving behind a vacancy. The former mechanism generally requires far lower energies than is necessary for displacement damage. From a radiation viewpoint, the total ionizing dose (TID) is a severe problem as it may increase to several hundred of kilorads during the lifetime of a

space mission. Ionization of the material creates free charge which can move in the material, either by drift or diffusion. In field-free neutral regions, carrier transport is dominated by thermal diffusion. The best known degradation effect of ionization damage is the occurrence of charge trapping by pre-existing or radiation-induced trap sites. Trapping implies the storage of charge for some time at a defect, which is released subsequently [32].

While the robust radiation tolerance of traditional III-V MODFETs is well-established [33], [34], we investigate the radiation tolerance of Si/SiGe MODFETs for the first time [8]. In this chapter, we study the DC and RF performance of Si/SiGe n-MODFETs irradiated with both X-rays and protons. The effects of radiation exposure on two major device design parameters (L_{SD} and L_G) in these T-gate Si/SiGe n-MODFET devices are examined. The underlying damage mechanisms for displacement damage and trap-generation in unrelaxed SiGe layers of n-MODFETs are also investigated using 2-D TCAD simulations.

3.2 Experimental Details

The DC characteristics of the devices were measured at room temperature using an Agilent 4155 Semiconductor Parameter Analyzer. Samples were wire-bonded into 28-pin DIP packages, and total ionizing dose radiation tests were performed at room temperature using 10 keV X-rays, at a dose rate of 540 rad SiO_2/s, to total doses as high as 5.4 Mrad SiO_2. Low energy proton exposure was also performed at room temperature using a 4 MeV proton beam at The Space Research Institute at Auburn University, at a dose rate of 1 krad SiO_2/s. The 4 MeV protons were used to better understand the impact of displacement damage on the buried Si/SiGe interfaces within the device. High energy proton exposure was performed at Crocker Nuclear Laboratory at University of California, Davis using a 63 MeV proton beam. A dose rate of 1.1 krad SiO_2/s was used

to expose these devices at room temperature. All terminals were grounded during all exposures. Table I summarizes the experimental test details. The DC characteristics of the devices were measured immediately after each cumulative dose was reached, and additional post-irradiation data were re-measured after approximately 120 hours to assess spontaneous self-annealing. An Agilent 8510C Vector Network Analyzer was used to extract S-parameters and RF metrics, both before and after irradiation (on-wafer RF measurements necessitate unpackaged passive exposure of devices).

Table 1: Radiation Exposure Details for three different radiation sources used.

Source Beam	Dose Rate (SiO2/s)	Temperature	Bias
10keV X-ray	540 rad	300K	Grounded
4 MeV Proton	1 krad	300K	Grounded
63 MeV Proton	1.1 krad	300K	Grounded

3.3 Radiation Response: DC Characteristics

Figure 21 shows typical I -V transfer characteristics as a function of X-ray dose for a 2-finger Si/SiGe n-MODFET with width and length dimensions of W/L = 10/0.08 and L_{SD} of 300 nm, after X-ray exposure. The gate current is not appreciably degraded.

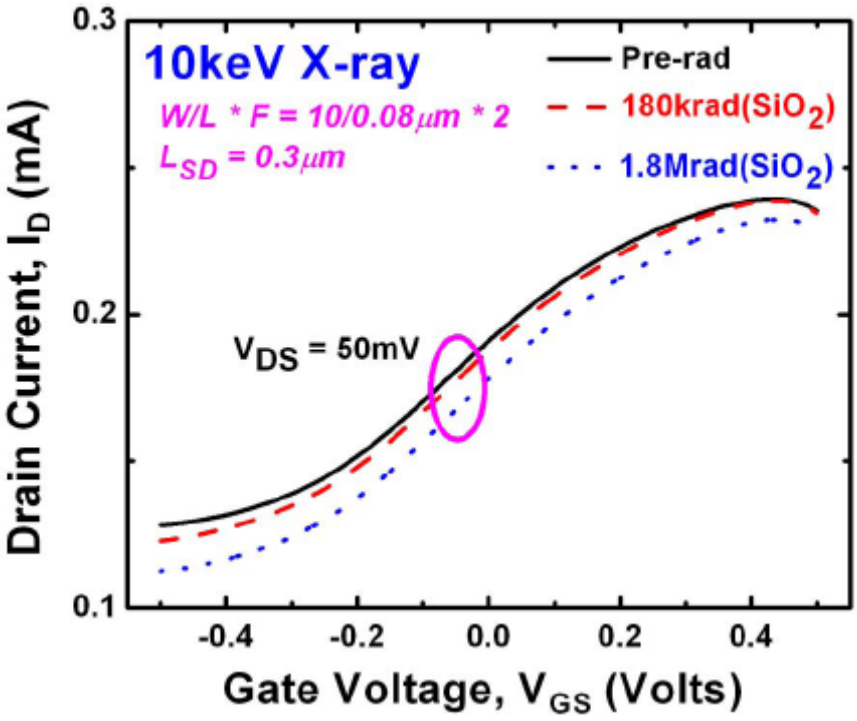

Figure 21: Impact of 10 keV X-ray irradiation on the transfer characteristics.

Figure 22 shows the output characteristics of a device with L_{SD} of 600 nm, indicating significant X-ray induced current degradation in saturation.

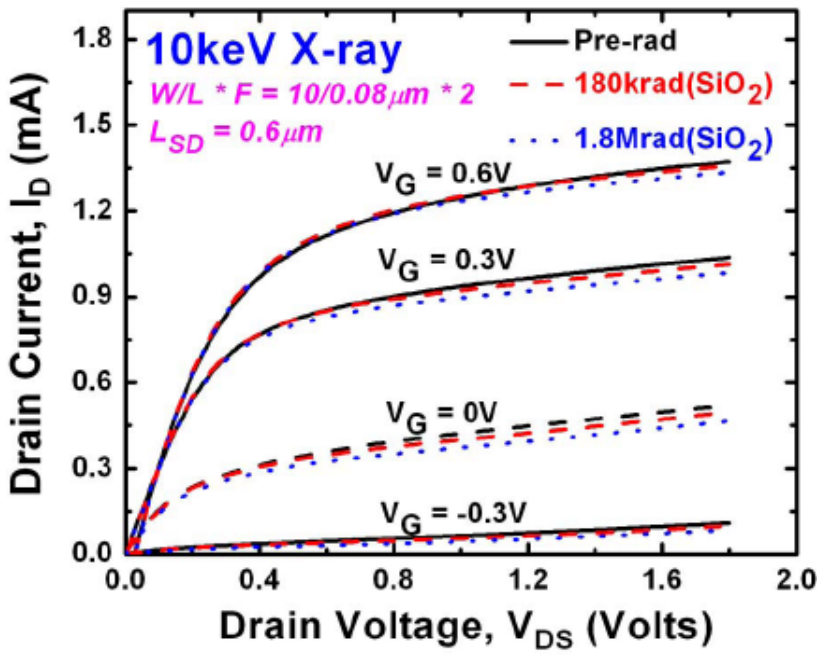

Figure 22: X-ray irradiation impact on the output characteristics.

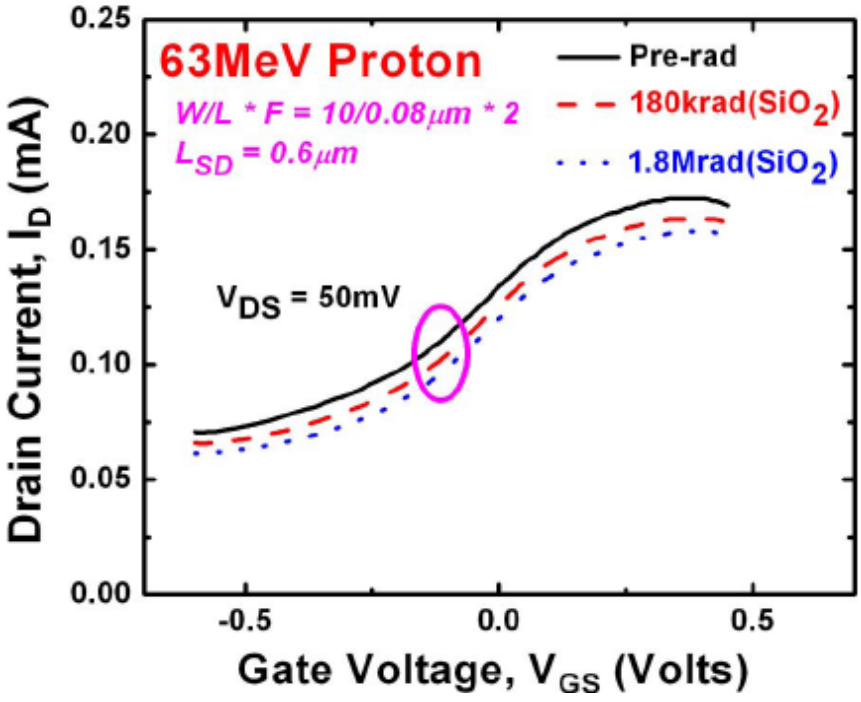

Figure 23: Impact of 63 MeV protons on transfer characteristics.

A similar trend in transfer characteristics is observed for 63 MeV proton irradiation of a device with L_{SD} of 600 nm and L_G of 80 nm, as shown in Figure 23.

The degradation trends are consistent in all the irradiated devices. Figure 24 shows the impact of low energy proton exposure on the transfer characteristics of a device with similar dimensions (the V bias is different). The degradation behavior of the transfer characteristics induced by the 4 MeV proton irradiation is attributed to the gate current change after irradiation, presumably due to displacement damage (Figure 24).

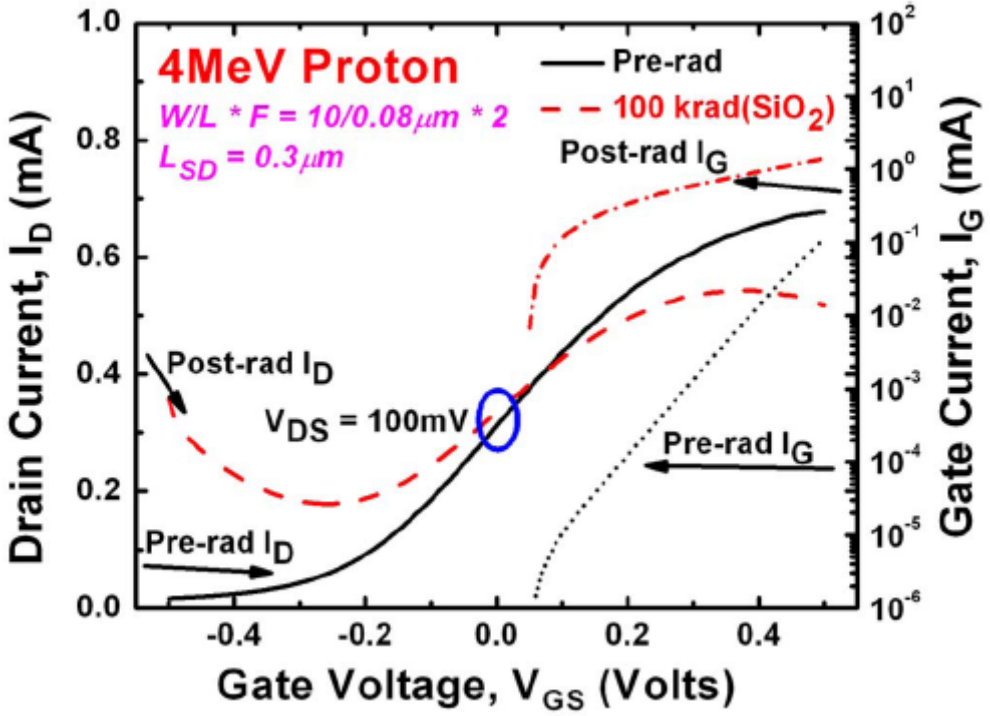

Figure 24: Impact of 4 MeV proton irradiation on the transfer characteristics.

Possible proton-induced displacement damage in the unrelaxed SiGe layer on top of the silicon channel can also reduce the electron confinement in the channel through strain relaxation, degrading the current drive. The excess off-state leakage current is shown in Figure 25, and following proton exposure increases with dose, presumably due to displacement damage effects.

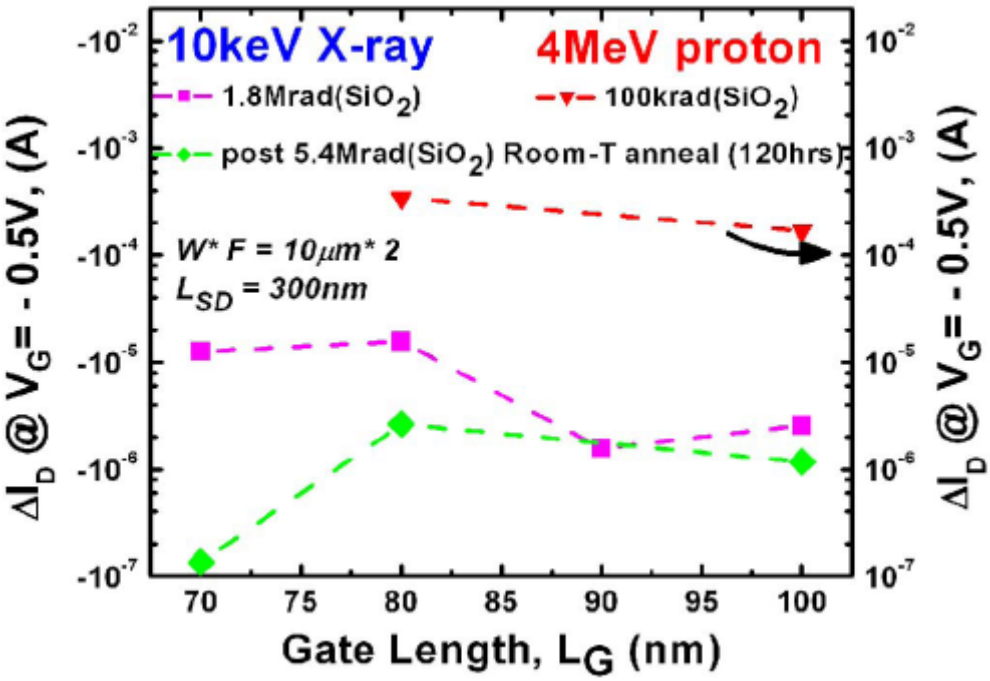

Figure 25: Impact of irradiation on off-state leakage current as a function of gate length.

An interesting *reduction* in leakage current is observed, however, following X-ray exposure (note that the left and right y-axes have different signs). It is interesting that the X-ray irradiation consistently reduces excess off-state leakage at room temperature. Detailed device simulation studies are presented in Section 2.5 to investigate the role of traps in Si/SiGe n-MODFETs and establish a correlation with observed radiation damage. Figure 26 shows the off-state leakage current degradation as a function of L_{SD} for devices with a fixed L_G = 80nm. Observe that the leakage recovery via X-ray exposure is more pronounced in devices with longer L_{SD}. A similar dependence on L_G and scaling is observed for the saturated drain current, as shown in Figures 27 and 28. Low energy protons clearly induce more damage in these devices compared to X-rays, at fixed total dose, suggesting the strong role of displacement damage.

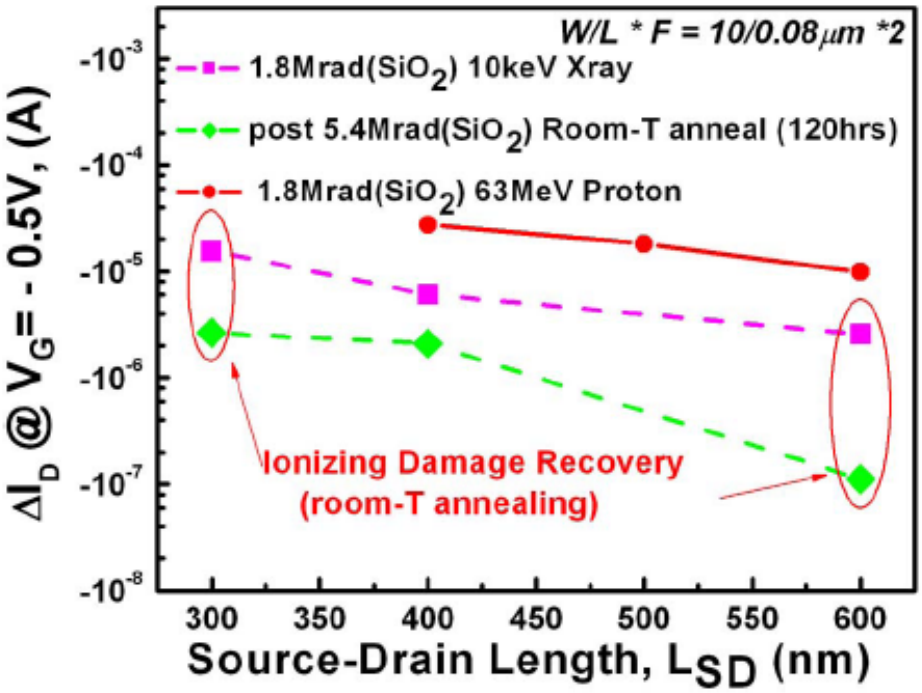

Figure 26: Variation of the X-ray and 63 MeV proton impact on off-state leakage with L_G.

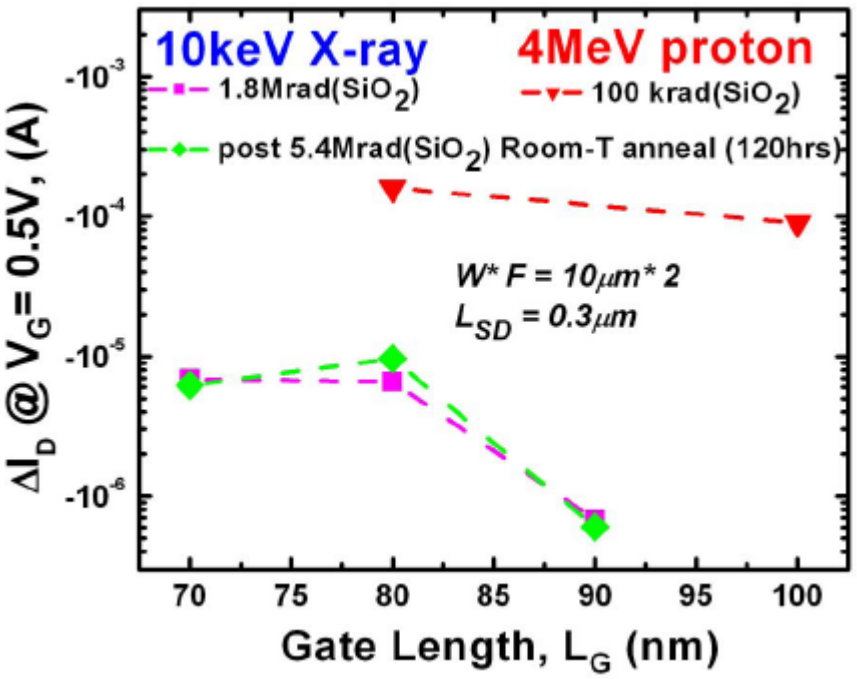

Figure 27: Impact of 10 keV X-ray and 4 MeV proton irradiation on the saturation current.

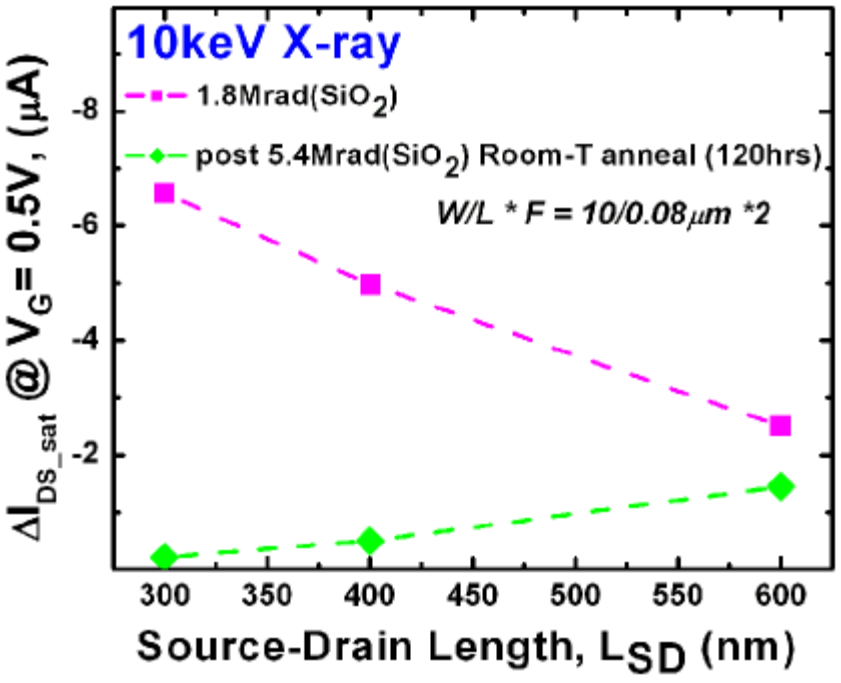

Figure 28: Variation of X-ray impact on the saturation current with L_{SD}.

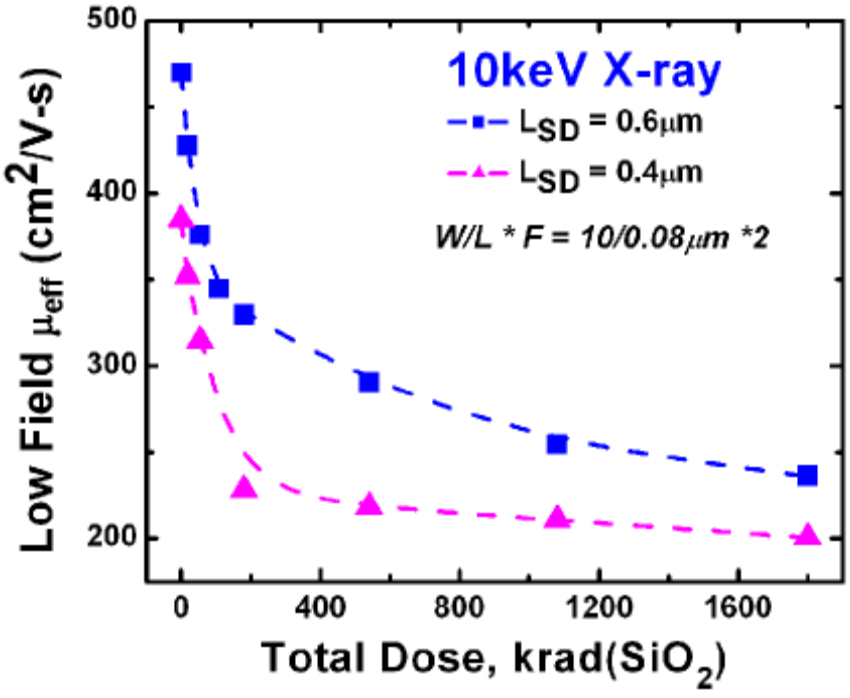

Figure 29: Low-field mobility degradation is observed after X-ray irradiation.

The low field effective mobility (μ_{eff}) was extracted for the devices with L_{SD} = 400nm and 600nm, and (W/L) x F = (10/0.08) x 2 (F is the number of gate fingers), prior to irradiation and as a function of total dose. From the I_D - V_{GS} and linear transconductance characteristics, the channel mobility was extracted from the slope of the quasi-linear function of $I_D/(g_m)^{1/2}$ vs. V_{GS}, which eliminates the mobility reduction factor of the source/drain series resistance [35]. Significant mobility degradation is observed at low total dose, saturating at higher total dose, as shown in Figure 29.

3.4 Radiation Response: RF Characteristics

Figure 30 shows the low energy proton induced cut-off frequency (f_T) degradation as a function of drain current. A 2.0 Mrad(SiO_2) passive exposure was performed for devices with L_{SD} = 300 nm and 600 nm, with (W/L) x F = (10/0.08) x 2. Devices with an L_{SD} of 600 nm show stronger peak f_T degradation compared to those with shorter L_{SD}, suggesting that larger displacement damage in the longer devices results in significant transconductance degradation.

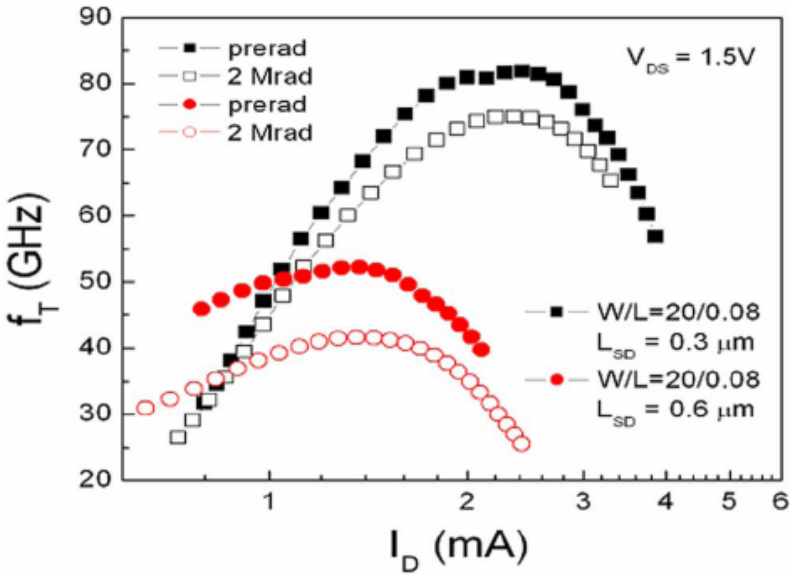

Figure 30: Cut-off frequency degradation with 4MeV proton passive exposure.

X-ray induced degradation in the RF characteristics is shown in Figure 31, after a 5.4 Mrad(SiO_2) exposure. No significant change in the peak f_T is observed, but about 10% degradation in peak f_{MAX} is observed. Interestingly, X-ray induced damage is also enhanced for the longer L_{SD} devices, as shown in Figure 32. Both peak f_T and peak f_{MAX} degrade by about 20% and 40%, respectively, for devices with longest of 800 nm.

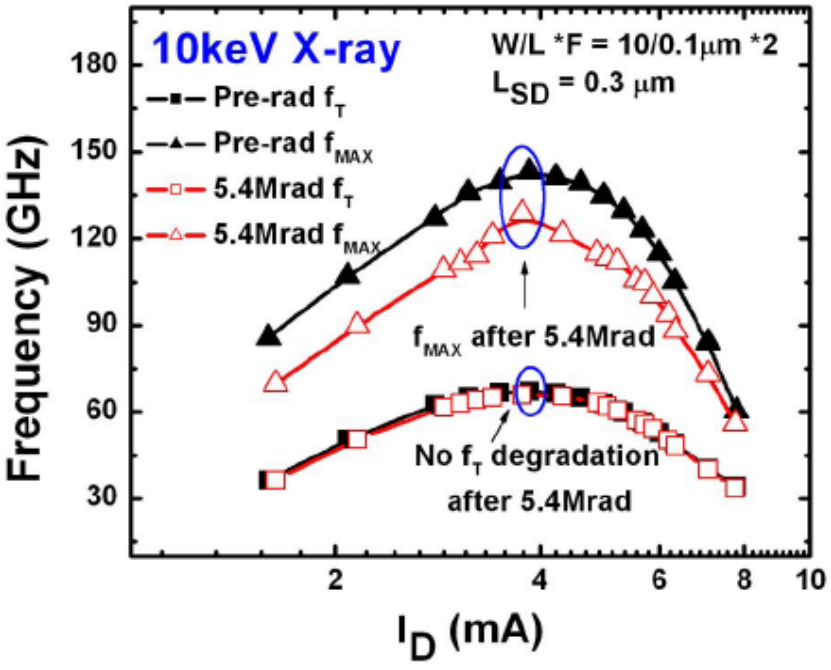

Figure 31: Degradation of RF characteristics after 10 keV X-ray passive exposure.

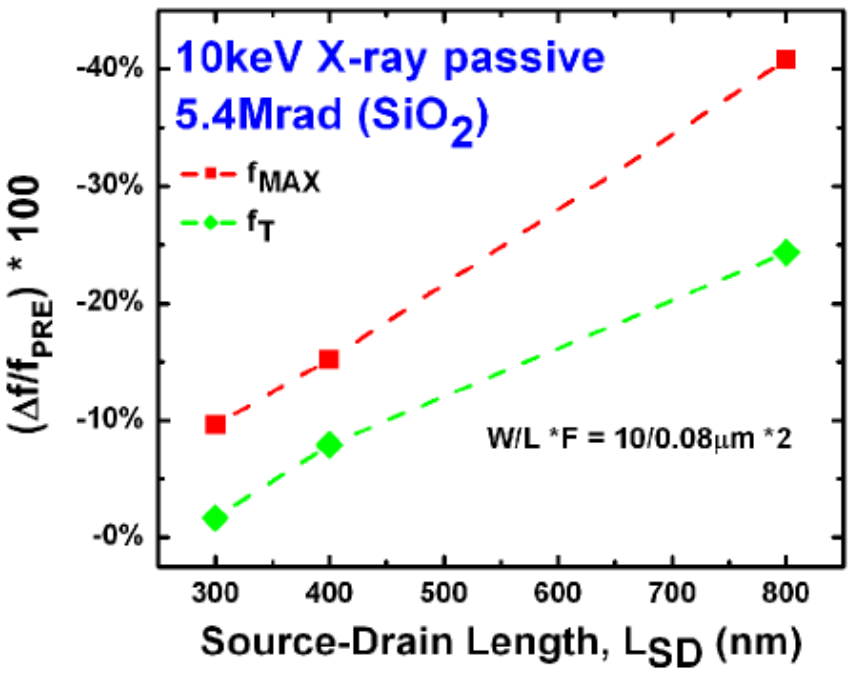

Figure 32: Higher degradation of RF characteristics is observed for longer L_{SD} devices.

3.5 TCAD Simulations

2-D device simulations are performed using the Sentaurus device simulator [36]. We use a boundary description tool to define the device structure and doping. The dependence of electron affinity and bandgap of strained-Si and SiGe on the mole fraction of germanium is considered to emulate the correct band-alignment for confinement of electrons. The electrons are confined in the thin strained silicon layer capped by SiGe on both sides, as shown in Figure 33. The metal gate contact is defined as a Schottky gate with a work-function of 4.3eV to obtain reasonably good transfer characteristics from simulations. The drift-diffusion model is used for simulation of carrier transport.

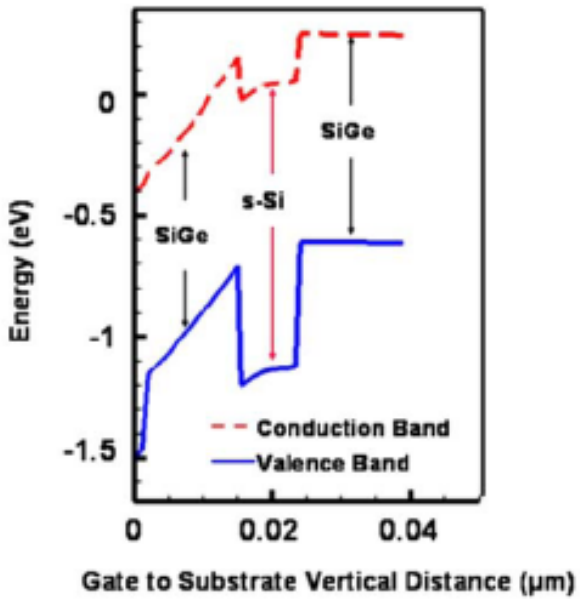

Figure 33: Simulated band-diagram of DUT along the vertical direction (gate to substrate).

Low energy proton induced displacement damage has been studied for GaN based HEMTs [37], [38]. The increase in gate current of SiGe MODFETs caused by 4 MeV low energy protons is attributed to displacement damage. Low energy protons produce higher damage in the top strained layers due to slower penetration than 63MeV high energy protons. The displacement damage, presumably in the unrelaxed SiGe layer, degrades the confinement of the electrons in the 2-D electron gas (2DEG) strained silicon channel, as depicted in Figure 34. The shift in CBO is attributed to the displacement damage induced strain relaxation. Simulations with a reduction in $CBO_{s\text{-}Si/SiGe}$, possibly induced by displacement damage, show an increase in I_G, as can be seen in Figure 35. These trends are in agreement with gate current experimental data (Figure 24).

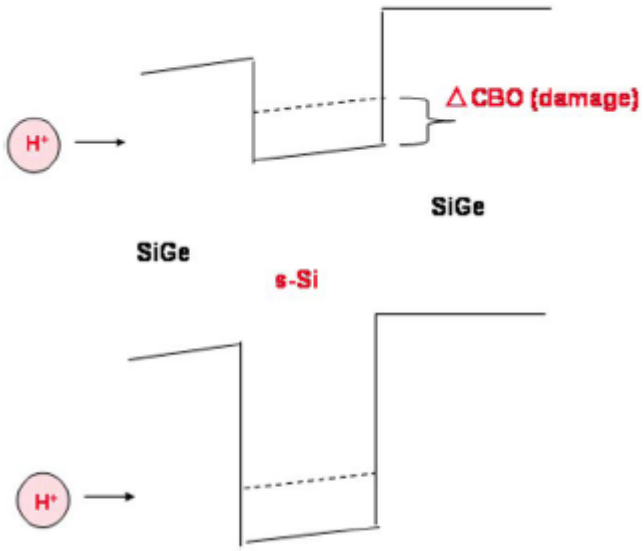

Figure 34: Displacement damage reduces the confinement of electrons in strained-silicon conduction band. The dashed line shows the conduction band offset after strain relaxation due to displacement damage.

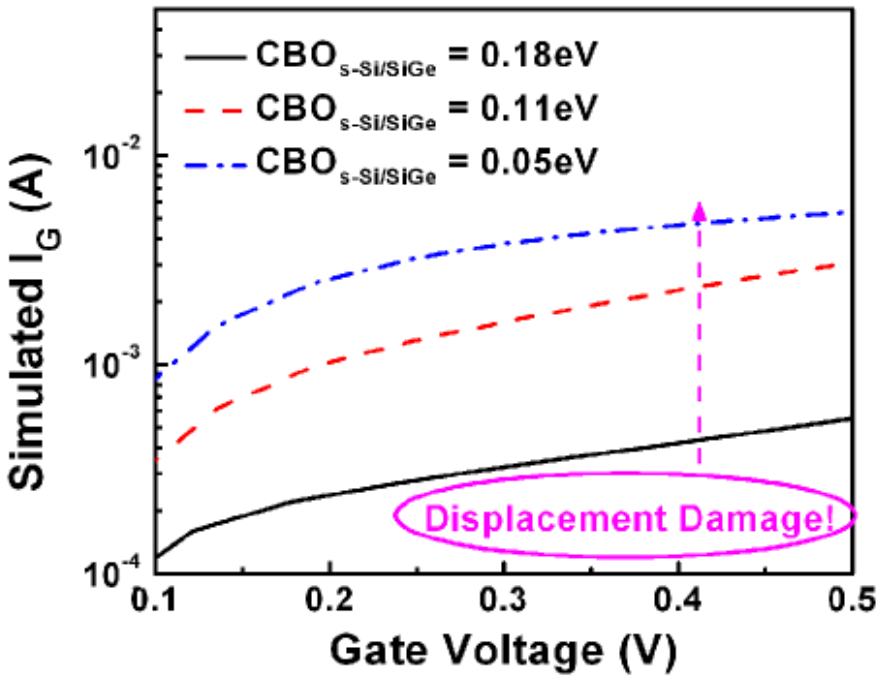

Figure 35: Simulated gate currents with lowering of $CBO_{s\text{-}Si/SiGe}$ show similar trends with experimental data (Figure 24).

The change in gate current (ΔI_G), especially at high drive current, increases with the lowering of the CBO. This is due to the presence of a favorable electric field for injection of electrons from the strained silicon channel into the SiGe confinement layer. As shown in Figure 36, ΔI_G increases with reduction in $CBO_{s\text{-}Si/SiGe}$.

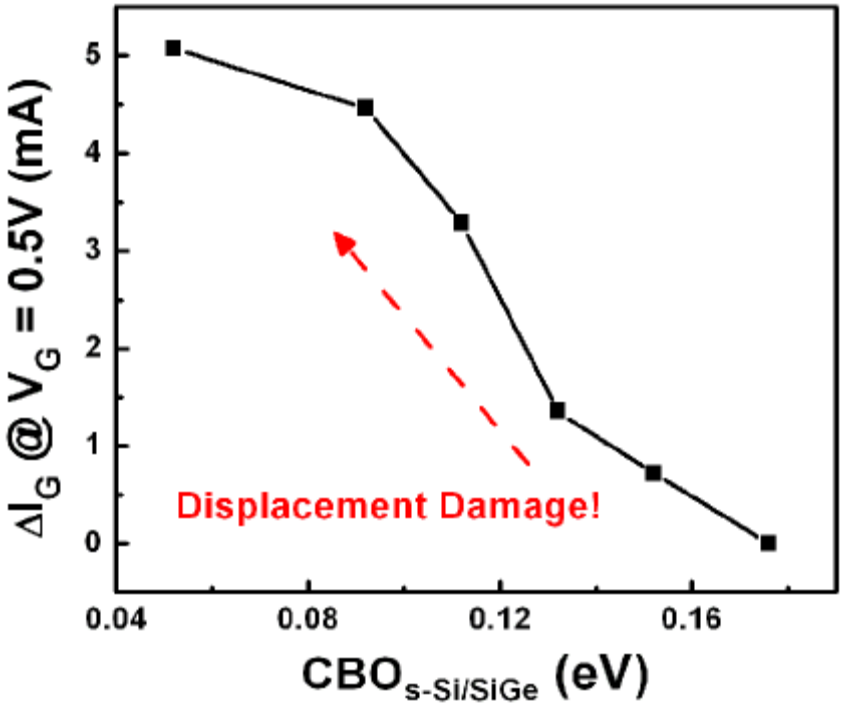

Figure 36: ΔI_G increases with change in conduction band offsets indicating higher displacement damage.

The SiGe layer on top of the strained-silicon channel is also strained, potentially resulting in a lower activation energy for trap formation via radiation exposure. We performed device simulations with bulk traps in this unrelaxed SiGe layer to investigate the impact of radiation-induced trap formation on n-MODFET characteristics. The Shockley–Read–Hall (SRH) recombination mechanism is taken into account while analyzing the role of traps [36]. In Figure 37, the simulated transfer characteristics with

bulk traps in the unrelaxed SiGe layer show trends in agreement with experimental data for the 63 MeV proton and 10 keV X-ray irradiated devices.

These observations are also consistent with the fact that radiation damage is more L_{SD} dependent than L_G dependent. A higher L_{SD} will have more volume of unrelaxed SiGe for generation of radiation-induced bulk traps. These results can also explain the observed room temperature annealing characteristics of the post-irradiated devices, presumably due to the spontaneous annealing of traps.

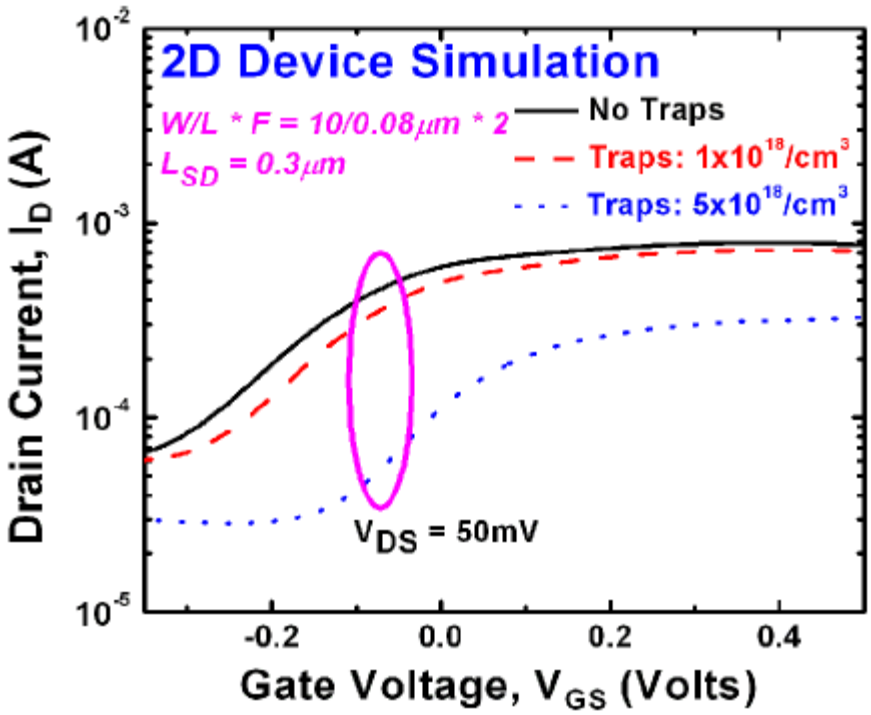

Figure 37: Simulated transfer characteristics of n-MODFETs with bulk traps introduced inside the SiGe cap layer.

CHAPTER 4

PROTON TOLERANCE OF SOI MOSFET

4.1 Introduction

In this chapter, we discuss the total ionizing damage in commercially available 65nm SOI CMOS technology [15]. Ionization damage in semiconductor devices is initiated when electron-hole-pairs (ehps) are generated along the track of secondary electrons emitted via photon-material interactions. Protons and other charged particles also generate ehps that lead to ionization damage. The total amount of energy deposited by a particle that results in ehp production is commonly referred to as total ionizing dose (TID). The typical unit of TID is rad, which denotes the energy absorbed per unit mass of a material. The possible physical processes leading to the creation of ionization defects are depicted in Figure 38 below. Since electrons have much higher mobility than holes in oxides, they are rapidly swept out of the dielectric [39].

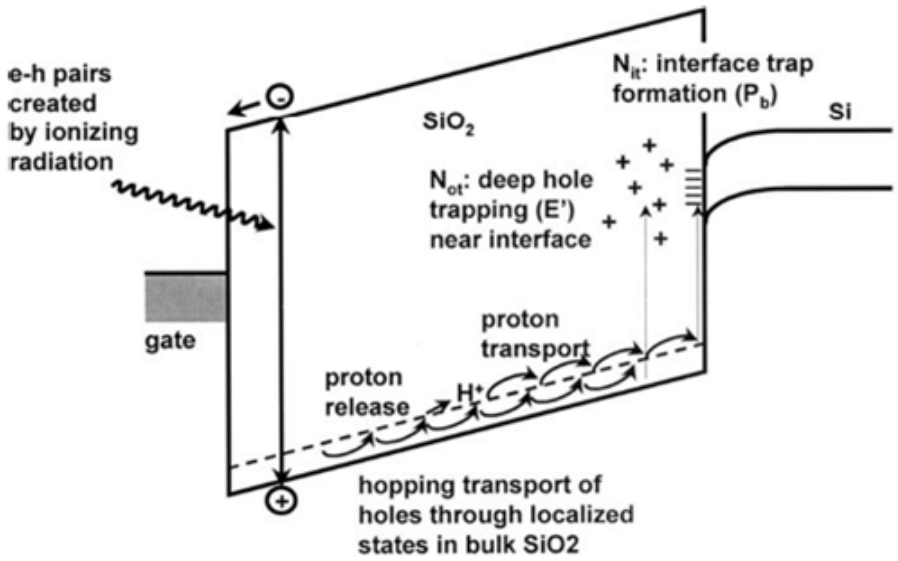

Figure 38: Major processes responsible for inducing TID damage in MOSFET [40].

In modern CMOS technologies, susceptibility of gate oxide to radiation-induced damage is reduced primarily due to the fact that defect buildup in gate oxides scales with t_{ox} [41]. Gate oxide hardness trends have continued to be observed in 0.25m (t_{ox} = 6nm), 0.18m (t_{ox} = 3.2nm), and 0.13m (t_{ox} = 2nm) respectively [42], [43]. However, defect buildup in thicker isolation oxides is the major cause of radiation-induced degradation in modern CMOS devices. The STI oxide thickness is typically greater than 300nm in advanced CMOS technologies. The thick buried oxide (BOX) in SOI technologies is also susceptible to radiation damage. However, for a 90nm SOI CMOS technology, a back-gate bias greater than 10V is required to observe any radiation damage induced front-gate threshold voltage shift.

The total dose radiation response of partially depleted SOI transistors has been investigated by using X-ray and proton sources in recent years [44], [45]. The proton tolerance of 0.18μm and 0.12μm bulk CMOS technology has been studied from both *dc* and *RF* standpoints [46], [47]. The thinner high quality gate oxides in aggressively scaled CMOS technologies exhibit reduced sensitivity to total dose radiation. Although the radiation tolerance of a 90nm SOI technology has been reported [48], the radiation response of advanced SOI CMOS technology from the viewpoint of RF performance under radiation has not been reported to date. The radiation tolerance of 65-nm SOI CMOS must be carefully scrutinized as a viable option for military and space applications. In this work, we examine the proton radiation response of the *dc* and *RF* characteristics of high speed devices in a state-of-the-art 65nm partially depleted SOI CMOS technology. Transconductance degradation and radiation induced threshold-voltage shift are used to assess the *dc* performance. S-parameters are used to characterize the *RF* performance of CMOS devices under proton radiation. We have restricted our analysis to total ionizing damage and not investigated radiation induced displacement damage and single event effects in this chapter. This work has been submitted for publication [49]

4.2 Experimental Details

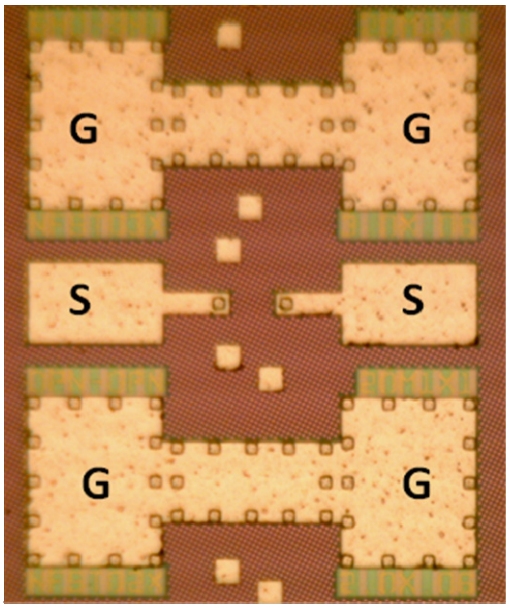

Figure 39: GSG Pad layout of 65nm SOI devices used for measurements.

The devices selected were laid out as multi-finger structures with GSG pad layout as shown in Figure 39, enabling high frequency measurements. An Agilent 4155C semiconductor parameter analyzer along with external bias-tees was used to perform *dc* device characterization at room temperature. Two port S-Parameter measurements upto 40GHz were performed on devices using an Agilent 8510C Vector Network Analyzer, both before and after irradiation (on-wafer RF measurements necessitate unpackaged passive exposure of devices). The conventional open-short de-embedding technique is used on raw S-Parameters of the devices to eliminate the effect of pad parasitics. All the measurements were performed at room temperature before and after the devices were exposed to proton radiation.

The samples were irradiated with 63 MeV protons at Crocker Nuclear Laboratory at University of California at Davis. A five-foil secondary emission monitor calibrated

against a Faraday cup is used for dosimetry measurements. The radiation source (Ta scattering foils) is located several meters upstream of the target. This establishes a beam spatial uniformity of about 15% over a 2.0 cm radius circular area. Beam currents from about 10nA to 50nA allow testing with proton equivalent gamma doses from 2MRad to 4.1MRad (SiO_2). The dosimetry system has been previously described and is accurate to about 10% [50]. A total of three samples, mounted on ceramic holders, were irradiated at different total dose of 2MRad, 3MRad and 4.1MRad. Each sample had same set of devices with different width and number of fingers. Since radiation damage can depend on the device bias conditions during exposure, the degradation results obtained here may not represent the worst case conditions.

4.3 Radiation Response: RF Characteristics

S-parameters are commonly used to characterize electrical response of high frequency transistors. After appropriate parasitic de-embedding, major RF figures-of-merit can be extracted from measured S-parameters. The cut-off frequency is extracted from S-Parameter measurements after de-embedding the pad parasitic through open and short structures. The 20dB/decade slope was extrapolated at 10GHz to facilitate extraction of f_T. Figure 40 shows typical f_T-V_{GS} curve for a 20-finger nFET with width and length dimensions (in μm) of W/L = 1/0.06. The impact of 63 MeV proton radiation is to degrade the cut-off frequency after a total dose of 2MRad. The degradation is pronounced around the common bias points of interest for RF applications i.e. peak-f_T region. This degradation not only reduces the maximum possible frequency of operation, but also causes a shift in bias to obtain small-signal current gain similar to pre-radiated device.

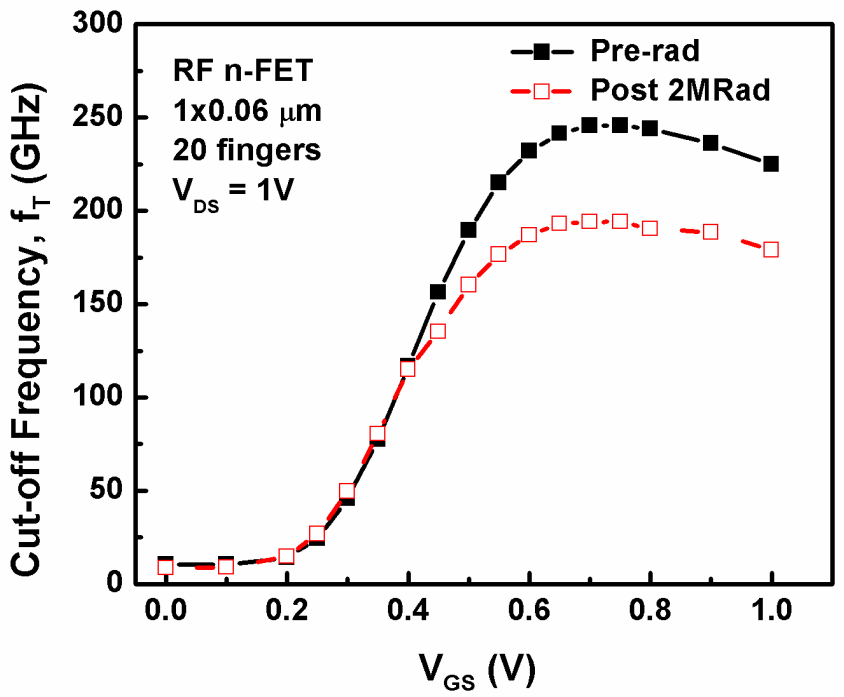

Figure 40: Proton radiation induced cut-off frequency degradation after total equivalent gamma dose of 2MRad (SiO_2).

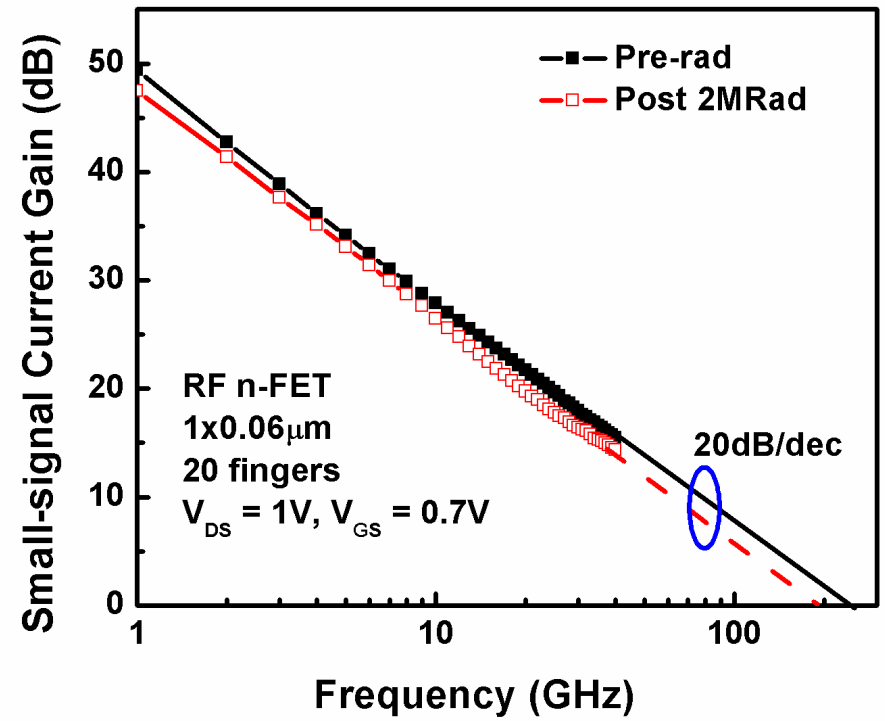

Figure 41: Degradation of small-signal current gain (h_{21}) in 60nm gate length n-MOSFET owing to proton radiation damage.

As shown in Figure 41, the peak cut-off frequency bias condition of V_{DS}=1.0V and V_{GS}=0.7V was used to calculate small-signal current gain (h_{21}). The gain for the same device is degraded after irradiation. Measurements were performed on a 40GHz VNA and linear extrapolation of 20dB/decade slope explains the shift in cut-off frequency (Figure 40) due to h_{21} degradation. The device transconductance degradation shown in Figure 42 is in harmony with the f_T degradation with bias.

The impact of proton irradiation on matching implications in RF circuits was analyzed using S-parameters. Previously, the impact of post-stressed enhanced gate leakage on RF matching has been studied from a reliability perspective [51]. To the best of author's knowledge, the impact of radiation on RF matching has been analyzed for the first time. It is shown in Figure 43 that the peak of f_T and f_{MAX} of a typical device is well-matched and occurs around V_{GS}=0.7V. Hence, we chose a bias point of V_{DS}=1.0V and V_{GS}=0.7V to analyze S-parameters for matching conditions.

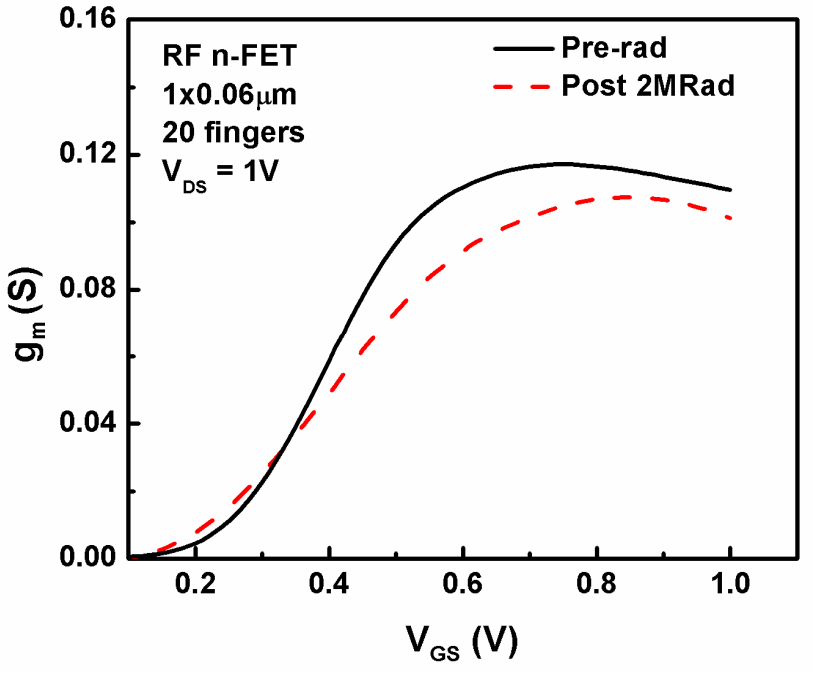

Figure 42: Transconductance (g_m) degradation plotted as a function of gate bias.

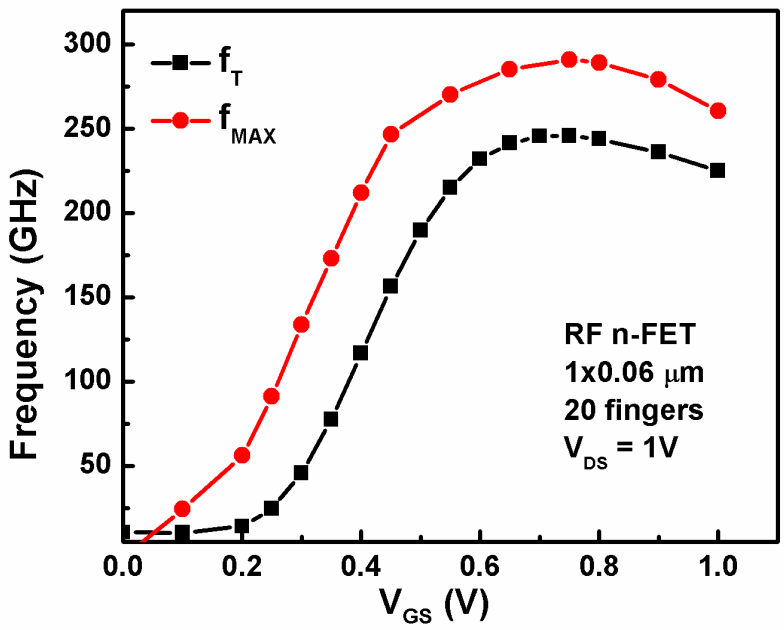

Figure 43: Closely matched f_T and f_{MAX} peaks in a typical 65-nm SOI nMOSFET.

In Figure 44, S_{11} shows negligible change upto a total equivalent gamma dose of 4.1MRad. We see that the S_{11} for the nFET always moves clockwise as frequency increases because S_{11} is the reflection coefficient corresponding to the input impedance when the output is terminated with the characteristic impedance Z_o. Notice here that the frequency was swept from 1GHz to 40GHz for S-parameter measurements. Since the capacitive part of input impedance is frequency dependent, the impact of enhanced leakage on current gain might diminish at high frequency [51]. S_{22} is essentially the output reflection coefficient looking back into the output port for a Z_o source termination. The radiation response of S_{22} showed minimal degradation in Figure 45 when radiated with a total equivalent gamma dose of 4.1MRad. Thus, input and output matching conditions are minimally impacted by proton radiation.

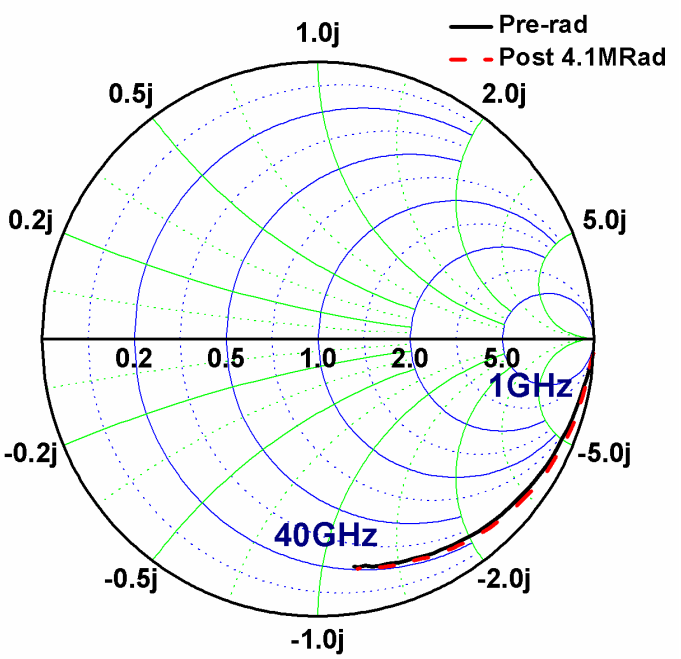

Figure 44: No significant change in S_{11} at a total dose of 4.1 MRad. The bias conditions are for peak f_T/f_{MAX} i.e. V_{DS} = 1V, V_{GS} = 0.7V.

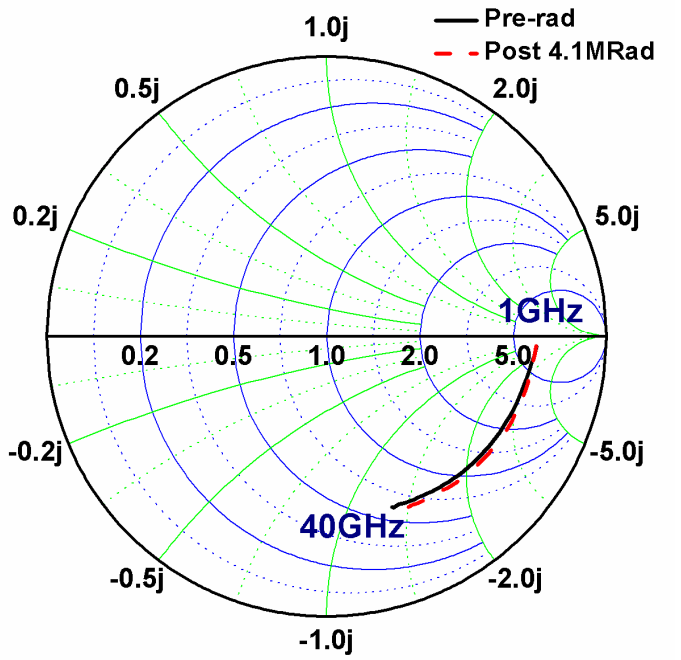

Figure 45: No significant change in S_{22} at peak f_T/f_{MAX} bias conditions.

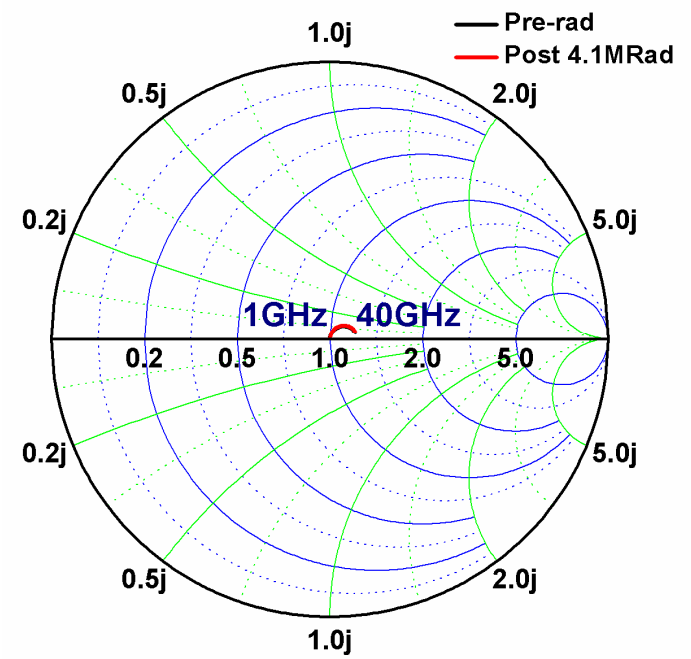

Figure 46: Reverse Gain, S_{12} shows no degradation at a total dose of 4.1MRad.

No radiation induced degradation can be observed for S_{12}, as shown in Figure 46. S_{12}, the reverse gain increases with increasing frequency.

From a RF CMOS standpoint, radiation induced f_T degradation was observed owing to device g_m degradation, presumably two most important RF figures of merit. However, matching conditions and reverse-gain experience negligible degradation, thus showing good tolerance to a total dose of 4.1MRad.

4.4 Radiation Response: DC Characteristics

Figure 47 shows the pre-radiation and post-radiation typical I_D-V_{GS} transfer characteristics for a 20-finger 65-nm nFET with drawn gate length of 60nm. It is clearly noticeable that the off-state leakage increases from 60pA to about 10µA in the linear region (V_{DS} = 50mV). This off-state leakage enhancement can be attributed to three reasons. Firstly, it can be attributed to the device region where the gate overlaps the

shallow trench isolation, where a parasitic inversion channel is produced at sufficiently high damage, resistively shunting the source to the drain. Charge trapped in the isolation dielectric, particularly at the Si/SiO_2 interface along the sidewalls of the trench oxide, creates the leakage path which becomes the dominant contributor to off-state drain to source leakage current in nFETs [52]. Secondly, it can be attributed to a floating body effect, sometimes referred to as "total-dose latch" or "snap back effect" [53]. However, a high level of drain current is observed for the lower V_{DS} of 50mV, well below that required to initiate impact ionization. Thus, we hesitate to call it a weak "total-dose latch" or "snap back effect", usually thought to be maintained or induced by impact ionization. Also, this effect is known to be more dominant in FD-SOI transistors [54], [55]. Thirdly, radiation defect buildup in the much thicker BOX layer could be the probable cause of *dc* parametric degradation. Since the source and drain implants in these partially-depleted devices reach upto the BOX, the back-gate conduction could be a source of leakage. This could lead to a increase in the floating body potential and cause a front-gate threshold shift in the device. Moreover, the pronounced leakage at V_{DS} = 1.0V can be attributed to either enhanced resistive shunting along the STI sidewalls or along the BOX surface, due to higher electric field between source and drain. These two competing leakage mechanisms need further investigation.

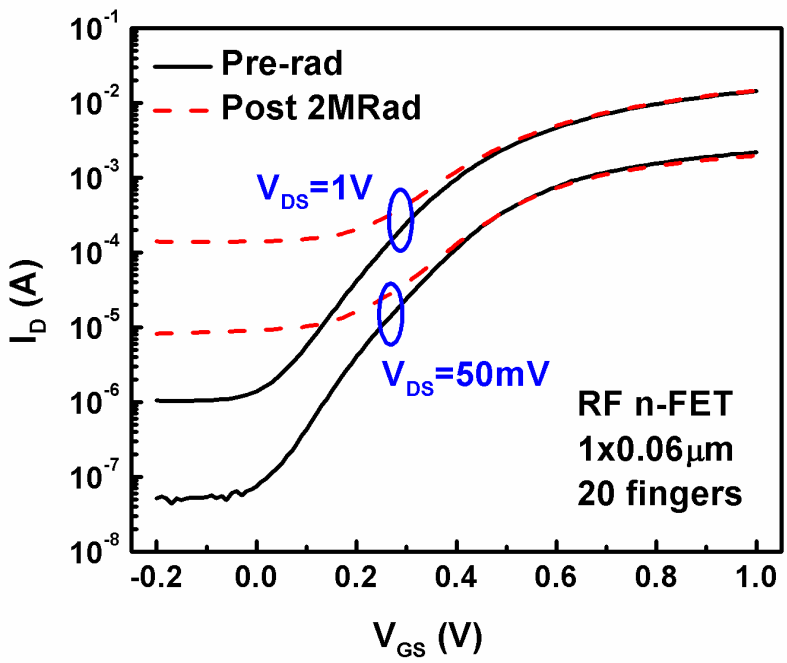

Figure 47: Transfer characteristics of a 65-nm n-MOSFET showing enhanced off-state leakage after irradiation.

The impact of proton irradiation on output characteristics of irradiated devices is shown in Figure 48. At high drain bias, the parasitic conduction paths enhance the total drain current and make the floating body effect more pronounced. Owing to high leakage enhancement and subthreshold slope degradation in the linear region, the linear transconductance of the device is also degraded in Figure 49. Even though this device technology has ultra-thin, high quality gate oxide, the impact of parasitic conduction along STI edges is easily noticeable in multiple finger devices, especially at a high total dose of 2MRad. The robustness of gate oxide to radiation induced damage is indicated by no change in gate current (I_G) as shown in Figure 50.

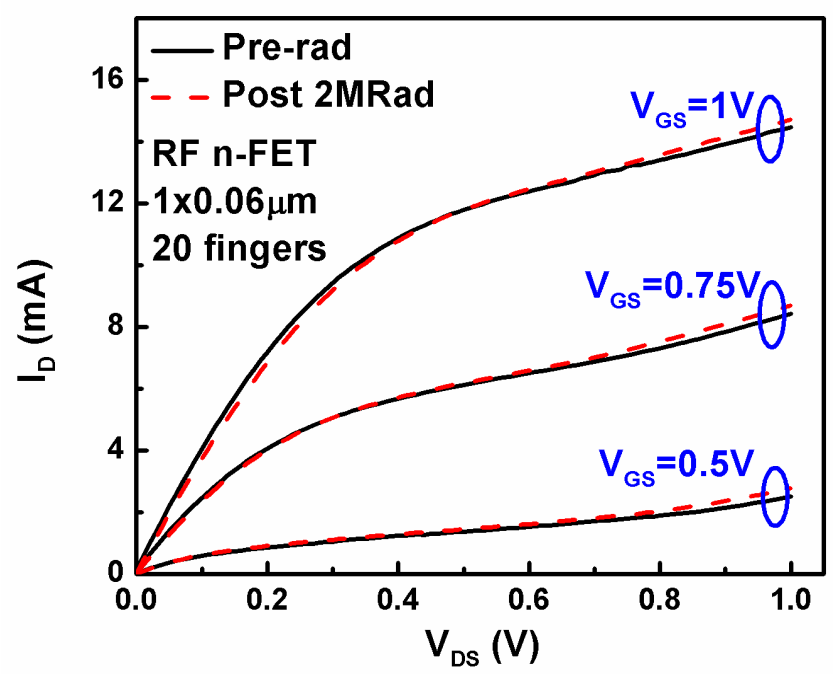

Figure 48: Output characteristics of the n-MOSFET showing enhanced body charging at high V_{DS} after irradiation.

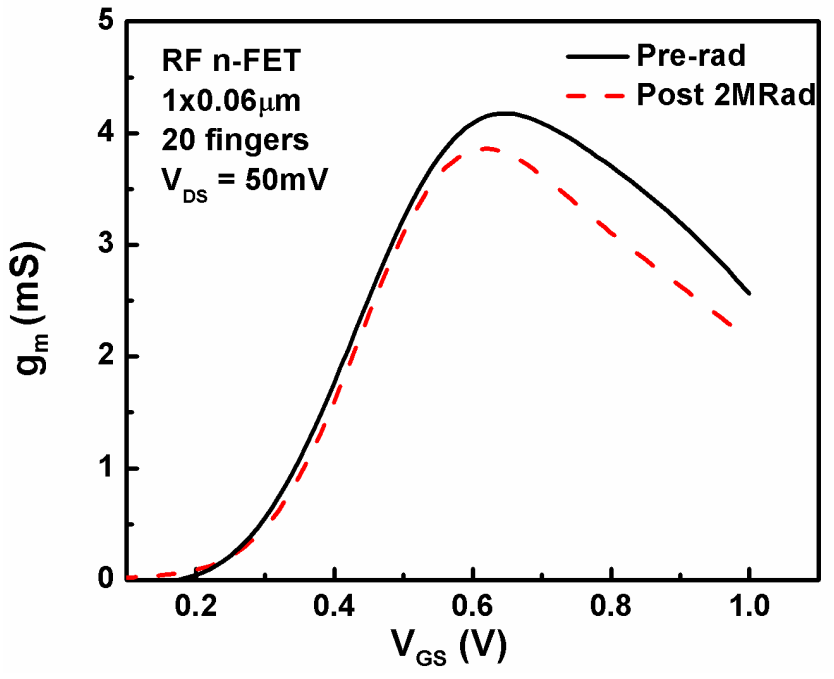

Figure 49: Degradation of linear transconductance of the device after irradiation.

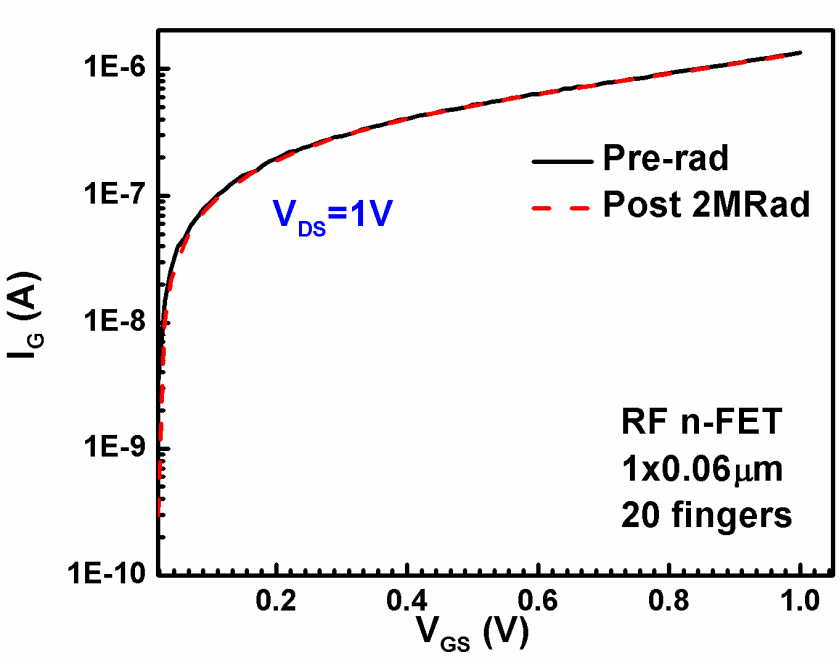

Figure 50: No significant change in gate current of the device was observed after 2MRad of total dose.

To understand the radiation-induced off-state leakage of nFETs more clearly, we extracted the threshold voltage (V_T) of all irradiated devices, both pre-radiation and post-radiation. The threshold voltage in the linear region was extracted as the gate voltage at a drain current of 40nA*(W/L) of the device. For our analysis, all devices are of the same drawn channel length of 60nm. As evident from Figure 47, the threshold voltage of the device is reduced post-radiation. Hence, we define change in radiation induced change in threshold voltage as $\Delta V_T = V_{T,\ pre} - V_{T,\ post}$. Figure 51 shows the total width (W*f) dependence of ΔV_T. The irradiated devices had total widths of 20μm, 40μm, 80μm, 90 μm and 120μm with different number of fingers in each device as indicated in Fig. 51. The highest threshold voltage shift was observed in two devices with W=1μm and f = 20 and 120, respectively.

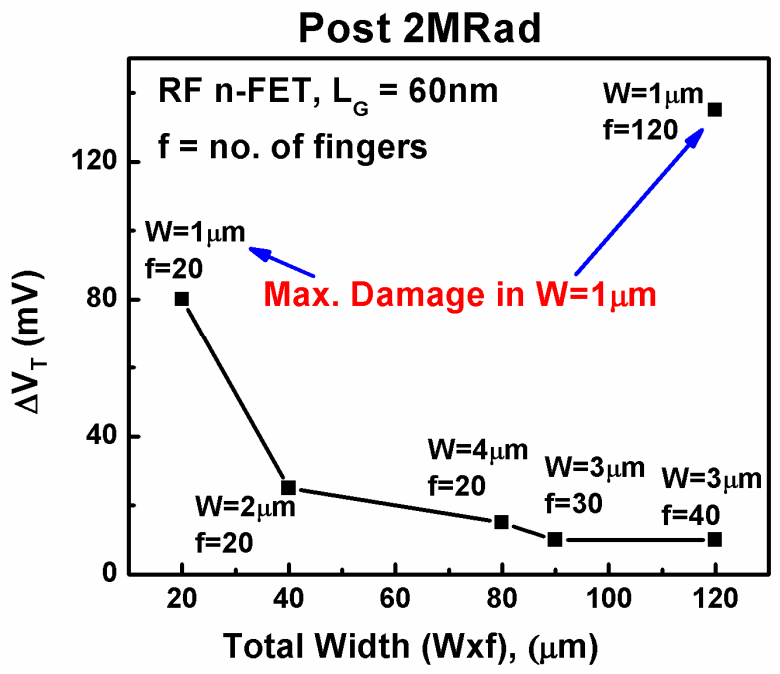

Figure 51: ΔV_T ($V_{T,\,pre}$ - $V_{T,\,post}$) dependence on total width of the devices.

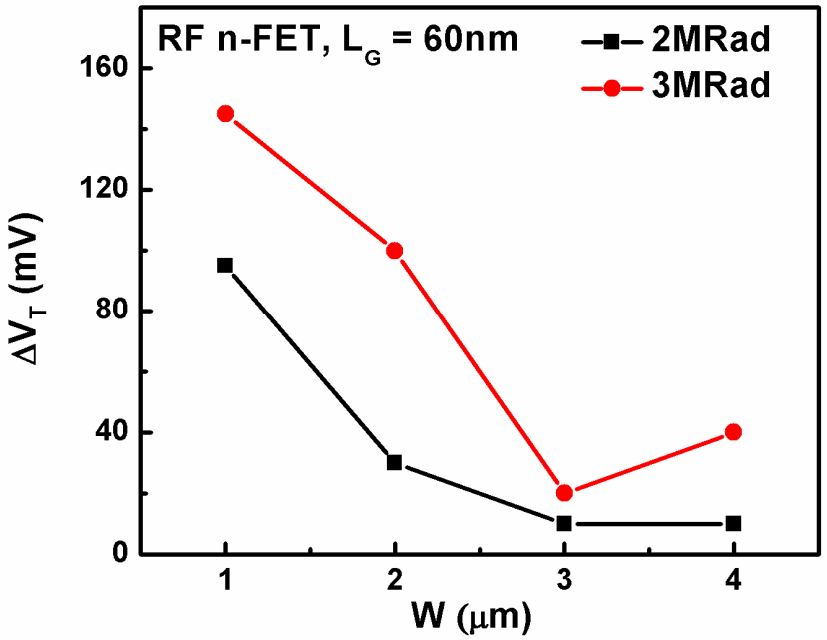

Figure 52: ΔV_T ($V_{T,\,pre}$ - $V_{T,\,post}$) dependence on width (W = total width/no of fingers) of the devices after both 2MRad and 3MRad total dose exposures.

This threshold voltage shift was found to multiply with number of fingers (f), when devices of same width were compared. In order to isolate the dependence of threshold voltage shift on width (W), we normalize the drain current of devices with number of fingers before reading the threshold voltage. The dependence of ΔV_T on device width (W = total width/f) is shown in Figure 52. A clear W dependence was observed, suggestive of STI induced parasitic conduction mechanism [56]. The effect of charge conduction on BOX surface is negligible compared to the effect of charge conduction along STI sidewalls.

CHAPTER 5

CONCLUSION

5.1 Conclusions

We have investigated the relevant physical mechanisms in SiGe MODFETs and SOI MOSFETs for RF and mixed-signal applications, particularly in extreme environments. DC and noise analysis were also used to understand the damage mechanisms in detail. Throughout this thesis, we have presented a thorough analysis of potential FET device technologies using *dc* and *ac* measurements and device simulations. By using careful device design and optimization, major hurdles for extreme environment operation of these devices can be overcome.

In Chapter 1, we reviewed the importance of RF and mixed-signal products in the fastest growing telecommunications market. The benefits offered by SiGe MODFETs and SOI MOSFETs for these applications were reviewed. We also explained the process and device architecture for both the technologies.

Chapter 2 concentrated on low-frequency noise in SiGe n-MODFETs. Different gate length and source-drain length splits were measured and the flicker noise bias dependence was correlated with the transconductance of the device to understand the underlying low-frequency noise mechanism. The channel resistance and source-drain resistance dominate in different drain-current regimes.

In Chapter 3, we analyzed the radiation tolerance of SiGe n-MODFETs using low energy protons, high energy protons and X-rays. Both *dc* and RF performance

degradation was observed, especially with low energy 4 MeV protons. Displacement damage and traps were investigated as underlying mechanism of radiation damage using TCAD simulations.

Finally in Chapter 4, state-of-the-art 65nm SOI CMOS technology was studied with an ionizing damage perspective using 63 MeV proton irradiation. Even though ultra-thin gate oxides are highly reliable, it was understood that STI sidewall-conduction enhanced the leakage current in n-MOSFET and also affected the RF performance. This effect was amplified in high width devices required for RF circuit design. However, no implications were found on RF matching of these devices as a result of proton irradiation. From a circuit designer's perspective, it is advisable to use higher width devices to maintain total ionizing radiation immunity. However, it comes at a cost of power-gain and noise figure since the optimal point is obtained at smaller widths.

5.2 Future Work

Apart from n-MODFETs, it is important to understand the low-frequency noise of their complementary counterparts (p-MODFETs) in detail. The buried-channel structures of both n-MODFETs and p-MODFETs can offer lower flicker noise compared to surface transport devices, thus providing lower phase noise in complementary circuits.

The role of interface traps at strained-Si/SiGe interface needs to be investigated. Current device simulation tools restrict the interface trap analysis to an oxide/semiconductor interface, thus making the analysis difficult. However, temperature can be used as a tool to probe the role of traps in these devices. We expect that cryogenic temperature measurements of these devices could provide more insight into the matter.

Also, pulsed I-V measurements could be interesting in the context of these devices with high germanium content. Since the thermal conductivity of germanium is much lower than silicon, we expect that the self-heating effects can be a major concern in these devices.

To confirm the role of STI sidewall leakage in n-MOSFET performance degradation, more biased radiation exposures are needed. It would be interesting to evaluate the radiation sensitivity of p-MOSFET in the same SOI CMOS technology platform since p-channel transistors are considered less prone to STI sidewall leakage.

REFERENCES

[1] JOSEPH, A.J., HARAME, D.L., JAGANNATHAN, B., COOLBAUGH, D., AHLGREN, D., MAGERLEIN, J., LANZEROTTI, L., FEILCHENFELD, N., ST. ONGE, S., DUNN, J., NOWAK, E., "Status and Direction of Communication Technologies-SiGe BiCMOS and RFCMOS," *Proc. IEEE,* vol. 93, no. 9, 2005.

[2] ISMAIL, K., "Si/SiGe high-speed field-effect transistors," *IEDM Tech. Dig.,* pp. 509-512, 1995.

[3] KONIG, U., GLUCK, M., HOCK, G., "Si/SiGe field-effect transistors," *J. Vac. Sci. Tech. B,* vol. 16, pp. 2609-2614, 1998.

[4] ENCISO, M., ANIEL, F., CROZAT, P., ADDE, R., ZEUNER, M., FOX, A., HACKARBATH, T., "0.3 dB minimum noise figure at 2.5 GHz of 0.13μm $Si/Si_{0.58}Ge_{0.42}$ n-MODFETs," *Electron. Lett.,* vol. 37, pp. 1089-1090, 2001.

[5] KOESTER, S.J., SAENGER, K.L., CHU, J.O., OUYANG, Q.C., OTT, J.A., JENKINS, K.A., CANAPERI, D.F., TORNELLO, J.A., JAHNES, C.V., STEEN, S.E., "Laterally scaled Si- $Si_{0.7}Ge_{0.3}$ n-MODFETs with $f_{MAX} > 200$ GHz and low-operating bias," *IEEE Electron Device Lett.,* vol. 26, no. 4, pp. 178-180, 2005.

[6] KOESTER, S.J., HAMMOND, R., CHU, J.O., "Extremely high transconductance $Ge/Si_{0.4}Ge_{0.6}$ p-MODFET's grown by UHV-CVD," *IEEE Electron Device Lett.*, vol. 21, no. 3, pp. 110-112, 2000.

[7] KOESTER, S.J., HAMMOND, R., CHU, J.O., MOONEY, P.M., OTT, J.A., PERAUD, L., JENKINS, K.A., WEBSTER, C.S., LAGNADO, I., DE LA HOUSSAYE, P.R., "SiGe p-MODFETs on silicon-on-sapphire substrates with 116GHz f_{max}," *IEEE Electron Device Lett.*, vol. 22, no. 2, pp. 92-94, 2001.

[8] MADAN, A., JUN, B., DIESTELHORST, R.M., APPASWAMY, A., CRESSLER, J.D., SCHRIMPF, R.D., FLEETWOOD, D.M., MARSHALL, P.W., ISAAC-SMITH, T., WILLIAMS, J.R., KOESTER, S.J., "The Proton Tolerance of Strained-Si/SiGe n-MODFETs," *IEEE Trans. Nucl. Sci.,* vol. 54, no. 6, pp. 2251-2257, 2007.

[9] OUYANG, Q.C., KOESTER, S.J., CHU, J.O., GRILL, A., SUBBANNA, S., HERMAN JR., D.A., "A Comprehensive Simulation Study of Strained-Si/SiGe nMODFET Scaling for RF Applications," *Proc. SISPAD*, pp. 59-62, 2002.

[10] TAKAGI, S., "Strained Si and SiGe-on-insulator MOSFETs for high performance/low power CMOS application," *Device Research Conference Tech. Dig*., pp. 37-40, 2002.

[11] GHANI, T., ARMSTRONG, M., AUTH, C., BOST, M., CHARVAT, P., GLASS, G., HOFFMANN, T., JOHNSON, K., KENYON, C., KLAUS, K., MCINTYRE, B., MISTRY, K., MURTHY, A., SANDFORD, J., SILBERSTEIN, M., SIVAKUMAR, S., SMITH, P., ZAWADSKI, K., THOMPSON, S., BOHR, M., "A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors," *IEDM Tech. Dig.*, pp. 979-980, 2003.

[12] NOWAK, E.J., ALLER, I., LUDWIG, T., KEUNWOO, K., JOSHI, R.V., CHUANG, C.-T., BERNSTEIN, K., PURI, R., "Turning silicon on its edge," *IEEE Circuits & Devices Mag.*, vol. 20, no. 1, pp. 20-31.

[13] PARK, C.-S., CHO, B.-J., KWONG, D.-L., "Thermally Stable Fully Silicided Hf-Silicide Metal-Gate Electrode", *IEEE Electron Device Lett.,* vol.25, no.6, pp. 372-374, 2004.

[14] VANDOOREN, A., THEAN, A.V.Y., DU, Y., TO, I., HUGHES, J., STEPHENS, T., HUANG, M., EGLEY, S., ZAVALA, M., SPHABMIXAY, K., BARR, A., WHITE, T., SAMAVEDAM, S., MATHEW, L., SCHAEFFER, J., TRIYOSO, D., ROSSOW, M., ROAN, D., PHAM, D., RAI, R., NGUYEN, B.-Y., WHITE, B., ORLOWSKI, M., DUVALLET, A., DAO, T., MOGAB, J., "Mixed-signal performance of sub-100nm fully-depleted SOI devices with metal gate, high K (HfO_2) dielectric and elevated source/drain extensions", *IEDM Tech. Dig.,* pp.975-977, 2003.

[15] LEE, W.-H., WAITE, A., NII, H., NAYFEH, H.M., MCGAHAY, V., NAKAYAMA, H., FRIED, D., CHEN, H., BLACK, L., BOLAM, R., CHENG, J., CHIDAMBARRAO, D., CHRISTIANSEN, C., CULLINAN-SCHOLL, M., DAVIES, D.R., DOMENICUCCI, A., FISHER, P., FITZSIMMONS, J., GILL, J., GRIBELYUK, M., HARMON, D., HOLT, J., IDA, K., KIENE, M., KLUTH, J., LABELLE, C., MADAN, A., MALONE, K., MCLAUGHLIN, P.V., MINAMI, M., MOCUTA, D., MURPHY, R., MUZZY, C., NEWPORT, M., PANDA, S.,

PEIDOUS, I., SAKAMOTO, A., SATO, T., SUDO, G., VANMEER, H., YAMASHITA, T., ZHU, H., AGNELLO, P., BRONNER, G., FREEMAN, G., HUANG, S.-F., IVERS, T., LUNING, S., MIYAMOTO, K., NYE, H., PELLERIN, J., RIM, K., SCHEPIS, D., SPOONER, T., CHEN, X., KHARE, M., HORSTMANN, M., WEI, A., KAMMLER, T., HONTSCHEL, J., BIERSTEDT, H., ENGELMANN, H.-J., HELLMICH, A., HEMPEL, K., KOERNER, G., NEU, A., OTTERBACH, R., REICHER, C., TRENTSCH, M., PRESS, P., FROHBERG, K., SCHALLER, M., SALZ, H., HOHAGE, J., RUELKE, H., KLAIS, J., RAAB, M., GREENLAW, D., KEPLER, N., "High performance 65 nm SOI technology with enhanced transistor strain and advanced-low-K BEOL," *Tech. Dig. IEDM,* pp. 56-60, 2005.

[16] LEE, S., KIM, J., KIM, D., JAGANNATHAN, B., CHO, C., JOHNSON, J., DUFRENE, B., ZAMDMER, L., WAGNER, L., WILLIAMS, R., FRIED, D., RIM, K., PEKARIK, J., SPRINGER, S., PLOUCHART, J., FREEMAN, G., "SOI CMOS Technology with 360 GHz fT NFET, 260 GHz fT PFET, and Record Circuit Performance for Millimiter-Wave Digital and Analog System-on-Chip Applications," *VLSI Technology Symp. Tech. Dig.,* pp. 54-55, 2007.

[17] WATANABE, T., "Low-noise operation in buried-channel MOSFETs," *IEEE Electron Dev. Letters*, vol. 6, no. 7, pp. 3170319, 1885.

[18] ANIEL, F., ENCISO-AGUILAR, M., ZEROUNIAN, N., CROZAT, P., ADDE, R., HACKBARTH, T., HERZOG, J.-H., and KONIG, U.. "High Speed Si/SiGe and Ge/SiGe MODFETs," *J. Fluid Mech.*, vol. 26, pp. 225–236, 1966.

[19] MADAN, A., CRESSLER, J.D., KOESTER, S.J., "Low-frequency Noise in Buried-Channel SiGe n-MODFETs," *Proc. Int'l SiGe Technology & Device Meeting,* 2008.

[20] GRAY, P.R., HURST, P.J., LEWIS, S.H., MEYER ,R.G., "*Analysis and Design of Analog Integrated Circuits"*, John Wiley & Sons, 4th ed.

[21] ALIEU, J., SKOTNICKI, T., JOSSE, E., REGOLINI, J.-L., BREMOND, G., "Multiples SiGe well: A new channel architecture for improving both NMOS and PMOS performances," *VLSI Symp. Tech. Dig.,* pp. 130-131, 2000.

[22] VON HAARTMAN, M., LINDGREN, A.C., HELLSTROM, P.E., MALM, B.G., ZHANG, S.L., OSTLING, M., "1/f noise in Si and $Si_{0.7}Ge_{0.3}$ pMOSFETs," *IEEE Trans. Electron Devices,* vol. 50, no. 2, pp. 2513-1519, 2003.

[23] OKHONIN, S., PY, A., GEORGESCU, B., FISCHER, H., RISCH, L., "DC and low-frequency noise characteristics of SiGe p-channel FET's designed for 0.13μm technology," *IEEE Trans. Electron Devices,* vol. 46, no. 7, pp. 1514-1517, 1999.

[24] TSUCHIYA, T., MATSUURA, T., MUROTA, J., "Low-frequency noise in $Si_{1-x}Ge_x$ p-channel metal-oxide-semiconductor field-effect transistors," *Jpn. J. Appl. Phys.,* vol. 40, no. 9A, pp. 5290-5293, 2001.

[25] LAMBERT, A.D., ALDERMAN, B., LANDER, R.J.P., PARKER, E.H.C., WHALL, T.E., "Low frequency noise measurements of p-channel $Si_{1-x}Ge_x$ MOSFET's," *IEEE Trans. Electron Devices,* vol. 46, no. 7, pp. 1484-1486, 1999.

[26] PREST, M.J., PALMER, M.J., BRAITHWAITE, G., GRASBY, T.J., PHILLIPS, P.J., MIRONOV, O.A., PARKER, E.H.C., WHALL, T.E., "Si/ $Si_{0.64}Ge_{0.36}$ /Si pMOSFET's with enhanced voltage gain and low 1/f noise,", *Proc. ESSDERC,* pp. 179-182, 2001.

[27] SONG, Y.J., LIM, J.W., MHEEN, B., KIM, S.H., BAE, H.C., KANG, J.Y., KIM, J.H., SONG, J.I., PARK, K.W., SHIM, K.H., "1/f noise in $Si_{0.8}Ge_{0.2}$ pMOSFETs under Fowler-Nordheim stress," *IEEE Trans. Electron Devices,* vol. 50, no. 4, pp. 1152-1156, 2003.

[28] JIANG, Y., LOH, W.Y., CHAN, D.S.H., XIONG, Y.Z., REN, C., LIM, Y.F., LO, G.Q., KWONG, D.-L., "Flicker Noise and Its Degradation Characteristics Under Electrical Stress in MOSFETs With Thin Strained-Si/SiGe Dual-Quantum Well," *IEEE Electron Dev. Letters,* vol. 28, no. 7, pp. 603-605, 2007.

[29] ZHAO, E., SUTTON, A.K., HAUGERUD, B.M., CRESSLER, J.D., MARSHALL, P.W., REED, R.A., EL-KAREH, B., BALSTER, S., YASUDA, H., "The Effects of Radiation on 1/f Noise in Complementary (npon + pnp) SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3243-49, 2004.

[30] VIKTOROVITCH, P., ROJO-ROMEO, P., LECLERCQ, J.L., LETARTRE, X., TARDY, J., OUSTRIC, M., GENDRY, M., "Low frequency noise sources in InAlAs/InGaAs MODFETs," *IEEE Trans. Electron Devices,* vol. 43, no. 12, pp. 2085-2100, 1996.

[31] VANDAMME, L.K.J., RIGAUD, D., PERANSIN, J.-M., ALABEDRA, R., DUMAS, J.-M., "1/f noise in MODFETs at low drain bias," *IEEE Trans. Electron Devices*, vol. 37, no. 10, pp. 2250-53, 1990.

[32] CLAEYS, C., SIMOEN, E., "*Radiation Effects in Advanced Semiconductor Materials and Devices"*, Springer-Verlag, 2002.

[33] LISTVAN, M.A., VOLD, P.J., ARCH, D.K., "Ionizing radiation hardness of GaAs technologies," *IEEE Trans. Nucl. Sci.,* vol. NS-34, no. 6, pp. 1664-1668, 1987.

[34] WEAVER, B.D., BOOS, J.B., PAPANICOLAOU, N.A., BENNETT, B.R., PARK, D., BASS, R., "High Radiation Tolerance of InAs/AlSb high-electron-mobility transistors," *Appl. Phys. Lett.,* vol. 87, pp. 173501-03, 2005.

[35] GHIBAUDO, G., "New method for the extraction of MOSFET parameters," *Elec. Lett.,* vol. 24, no. 9, pp. 543-545, 1988.

[36] "Sentaurus Device Manual Version Y-2006.06," Synopsys Inc.

[37] WHITE, B.D., BATAIEV, M., BRILLSON, L.J., CHOI, B.K., FLEETWOOD, D.M., SCHRIMPF, R.D., PANTELIDES, S.I., DETTMER, R.W., SCHAFF, W.J., CHAMPLAIN, J.G., MISHRA, A.K., "Characterization of 1.8-MeV proton-irradiated AlGaN/GaN field-effect transistor structures by nanoscale depth-resolved luminescence spectroscopy,", *IEEE Trans. Nucl. Sci.,* vol. 49, no. 6, pp. 2695-2701, 2002.

[38] KARMARKAR, A.P., JUN, B., FLEETWOOD, D.M., SCHRIMPF, R.D., WELLER, R.A., WHITE, B.D., BRILLSON, L.J., MISHRA, U.K., "Proton irradiation effects on GaN-based high electron-mobility transistors with Si-doped $Al_xGa_{1-x}N$ and thick GaN cap layers," *IEEE Trans. Nucl. Sci.,* vol. 51, no. 6, pp. 3801-3806, 2004.

[39] OLDHAM, T.R., "Switching oxide traps," *Radiation Effects and Soft Errors in Integrated Circuits and Electronic Devices,* R.D. Schrimpf and D.M. Fleetwood, Eds. Singapore: World Scientific, 2004.

[40] MCLEAN, F.B., OLDHAM, T.R., "Basic mechanisms of radiation effects in electronic materials and devices," *Harry Diamond Lab. Tech. Rep.*, vol. HDL-TR, pp. 2129, 1987.

[41] TAUR, Y., NING, T.H., "*Fundamental of Modern VLSI Devices"*, New York: Cambridge Univ. Press, 1998.

[42] LACOE, R.C., MAYER, D.C., OSBORN, J.V., YABIKU, G., "Total dose hardness of three commercial CMOS microelectronic foundries," *Proc. 4th RADECS,* pp. 265-270, 1997.

[43] LACOE, R.C., "CMOS scaling design principles and hardening by design methodology," *NSREC Short Course,* 2003.

[44] LI, Y., NIU, G., CRESSLER, J.D., PATEL, J., MARSHALL, P.W., KIM, H.S., LIU, M.S.T., REED, R.A., PALMER, M.J., "Proton Radiation Effects in 0.35μm Partially Depleted SOI MOSFETs fabricated on UNIBOND", *IEEE Trans. Nucl. Sci.*, vol. 49, no.6, pp. 2930-36, 2002.

[45] FARLET-CAVROIS, V., COLLADANT, T., PAILLET, P., LERAY, J.L., MUSSEAU, O., SCHWANK, J.R., SHANEYFELT, M.R., PELLOIE, J.L., PONCHARRA, J., "Worst-case bias during total dose irradiation of SOI transistors," *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 2183–2188, 2000.

[46] LI, Y., CRESSLER, J.D., LU, Y., PAN, J., NIU, G., REED, R.A., MARSHALL, P.W., JOSEPH, A.J., "Proton Tolerance of Multiple-Threshold Voltage and Multiple-Breakdown Voltage CMOS Device Design Points in a 0.18μm System-on-a-Chip CMOS Technology," *IEEE Trans. Nucl. Sci.,* vol. 50, no. 6, pp. 1834-1838, 2003.

[47] VENKATARAMAN, S., HAUGERUD, B.M., ZHAO, E., BANERJEE, B., SUTTON, A.K., MARSHALL, P.W., LO, C.-H., CRESSLER, J.D., LASKAR, J., PAPAPOLYMEROU, J., JOSEPH, A.J., "Impact of Proton Irradiation on the RF Performance of 0.12μm CMOS Technology," *Proc. IRPS,* pp. 356-359, 2005.

[48] APPASWAMY, A., JUN, B., DIESTELHORST, R.M., ESPINEL, G., PRAKASH, A.P.G., CRESSLER, J.D., MARSHALL, P.W., MARSHALL, C.J., LIANG, Q., FREEMAN, G., ISAACS-SMITH, T., WILLIAMS, J.R., "The Effects of Proton Irradiation on 90nm Strained Si CMOS on SOI Devices", *IEEE Radiation Effects Data Workshop*, pp. 62-65, 2006.

[49] MADAN, A., PHILLIPS, S.D., CRESSLER, J.D., MARSHALL, P.W., LIANG, Q., FREEMAN, G., "Impact of Proton Irradiation on RF Performance of 65nm SOI CMOS Technology," *RADECS 2008* (Submitted).

[50] MARSHALL, P.W., DALE, C.J., CARTS, M.A., LABEL, K.A., "Particle-induced bit errors in high performance fiber optic data links for satellite data management", *IEEE Trans. Nucl. Sci.,* vol. 41, no. 6, pp. 1958-1965, 1994.

[51] PANTISANO, L., CHEUNG, K.P., "The Impact of Post Breakdown Gate Leakage on MOSFET RF Performances", *IEEE Electron Dev. Lett.,* vol. 22, no. 12, pp. 585-587, 2001.

[52] SHANEYFELT, M.R., DODD, P.E., DRAPER, B.L., FLORES, R.S., "Challenges in hardening technologies using shallow-trench isolation," *IEEE Trans. Nucl. Sci.,* vol. 45, pp. 2584-2592, 1998.

[53] FERLET-CAVRIOS, V., QUOIZOLA, S., MUSSEAU, O., FLAMENT, O., LERAY, J.L., PELLOIE, J.L., RAYNAUD, C., FAYNOT, O., "Total dose induced latch in short channel NMOS/SOI transistors," *IEEE Trans. Nucl. Sci.,* vol. 45, no. 6, pp. 2458-2466, 1998.

[54] FLAMENT, O., TORRES, A., FERLET-CAVROIS, V., "Bias Dependence of FD Transistor Response to Total Dose Irradiation," *IEEE Trans. Nucl. Sci.,* vol. 50, no. 6, pp. 2316-2321, 2003.

[55] SCHWANK, J.R., SHANEYFELT, M.R., DODD, P.E., BURNS, J.A., KEAST, C.L., WYATT, P.W., "New Insights into Fully-Depleted SOI Transistor Response After Total-Dose Irradiation," *IEEE Trans. Nucl. Sci.,* vol. 47, no.3, pp. 604-612, 2000.

[56] BRADY, F.T., MAIMON, J.D., HURT, M.J., "A Scalable, Radiation Hardened Shallow Trench Isolation," *IEEE Trans. Nucl. Sci.,* vol. 46, no. 6, pp. 1836-1840, 1999.